RediSem Passive PFC - LED Driver Design Guide

Overview

RediSem Patented Passive Power Factor Control (PPFC) LED driver designs offer significant performance benefits over standard LED driver solutions. They use a unique single stage series-resonant converter with a charge-pump PFC circuit to give good power factor correction. These driver designs are flicker free and are much lower cost than a 2-stage conventional design. RediSem's resonant converters designs are highly efficient and have low Electromagnetic Interference (EMI) while offering a cost-competitive solution through the use of bipolar transistors and a high level of IC integration with Control IC's such as the RED2401, RED2501 & RED2511. In summary the key features and benefits are:

- **RediSem Single Stage LED converter:**
  - Charge-pump PFC circuit
  - Low output current ripple
  - High efficiency
  - Low EMI
  - Constant Current Output
  - Bipolar transistor half-bridge

- **RediSem's LED Controller ICs:**
  - Primary-Side Regulation (PSR) +/-5% constant current regulation
  - No-load output voltage protection to meet SELV
  - Short-circuit protection
  - OTP (over-temperature) protection
  - Integrated bipolar transistor drive circuit
  - SO8 package or SOT23-6

This design guide's aim is to explain the use of RediSem's controller ICs and LED driver application so that you can develop your own designs. It is recommended you always use one of RediSem's example designs as a starting point for new designs. Please check with us regularly for updates and additional information. As RediSem develops more LED driver example designs, this Design Guide will be updated from time to time.

Top-level Design Notes

Topology

The design described here combines a fully resonant half-bridge converter with integral Charge Pump Power Factor Correction to deliver a low cost product which is fully EMI compliant at a fraction of the cost of competing solutions.

Series-Resonant Half-Bridge

The series-resonant half-bridge is ideally suited to LED Driver applications, because it provides excellent efficiency and has inherently good immunity and low-noise characteristics to make EMC compliance very easy. RediSem's LED Driver Controller ICs are specifically designed for series-resonant topologies for LED Drivers. RediSem's controller ICs are unique in that they combine a self-oscillating bipolar converter (CSOC) topology with a simple half-bridge control scheme using bipolar switching devices, which are both lower cost and more robust than MOSFET alternatives. Furthermore, the self-oscillating design is inherently immune to running in capacitive mode, which is a considerable problem for MOSFET-based solutions.

Charge Pump Power Factor Correction

Most countries now require that the line inputs of lighting appliances comply with power factor and harmonic emissions. The requirements vary from country to country and also depend upon various parameters including input power and intended use. With few exceptions, LED Drivers need some form of Power Factor Correction (PFC) in order to comply with limits for Power Factor and Harmonic Emissions. One solution has been to use Active Power Factor Correction (APFC) which requires a separate switching Power Factor Correction block, with dedicated switching device and control circuit. While this two-stage approach is effective at delivering good power factor correction and harmonic suppression, the resulting production cost is high and relatively uncompetitive. The RediSem Charge Pump PFC topology uses switching diodes to provide charge-pumping (boosting) to achieve control of Power Factor and Harmonic Emissions, without the need for another controller or any additional active switching devices.

Integrated CSOC and Charge Pump PFC

Figure 1 shows the topology of RediSem's LED Driver which integrates RediSem's CSOC with the Charge Pump PFC topology. The Charge Pump PFC stage is fitted in the return current path, between the main transformer primary winding and the diode bridge block. The primary winding current drives the boosting and power factor correction.

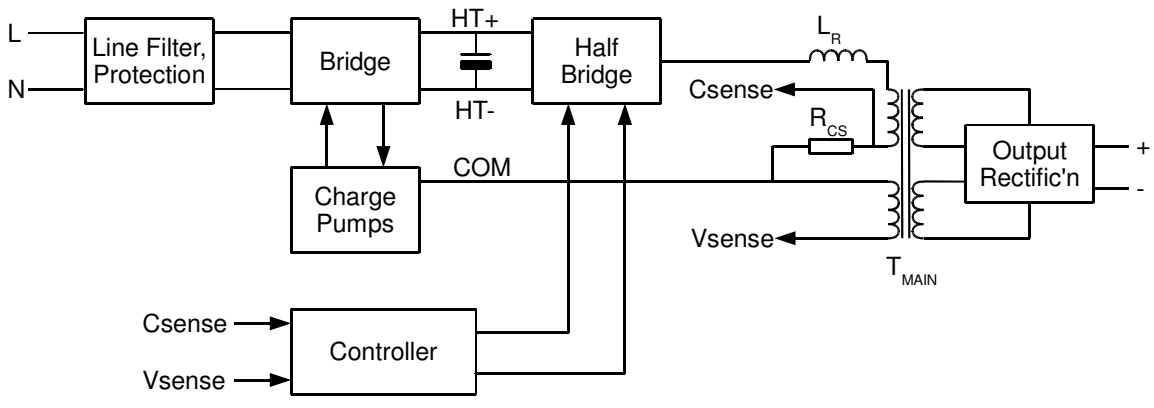

Figure 1: CSOC plus Charge Pump PFC

Using CSOC with Active Power Factor Correction (APFC)

For some applications, such as those with very wide input/output voltage requirements, it may be necessary to use Active Power Factor Correction (APFC). RediSem's LED controller IC's may be easily combined with a third-party PFC pre-regulator design, as shown in Figure 2. Please consult AN2111 for APFC design information.

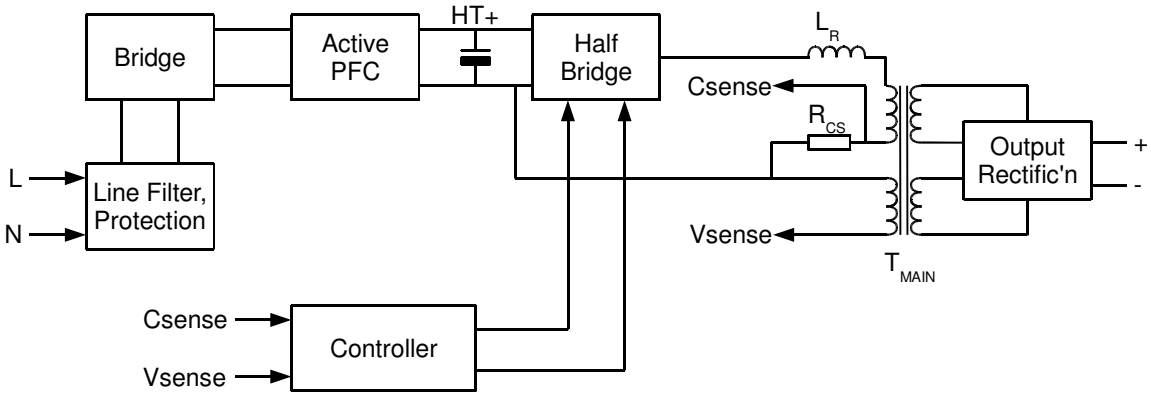

Figure 2: CSOC with Active PFC

Charge Pump Power Factor Correction Explained

A simplified example of a LED driver with a single charge pump PFC stage is shown in Figure 3. Here, the circulating primary current flows through primary of transformer **T_{MAIN}** and the resonant tank **C_R** and **L_R**. Ignoring the boost capacitor **C_{BOOST}** for a moment, this AC switching current would flow through **D_{PUSH}** and **D_{PULL}** alternately (shown by looped arrows in Figure 3) thereby pumping current into the bulk capacitor **C_{HT}**, boosting its voltage higher than the voltage on **C_{F2}**. Capacitor **C_{BOOST}** acts as a low-pass filter, reducing the rise time of the voltage waveform across it, so that the amount of current pumped depends on the switching frequency, the value of **C_{BOOST}** and the difference between the voltages of capacitors **C_{HT}** and **C_{F2}**.

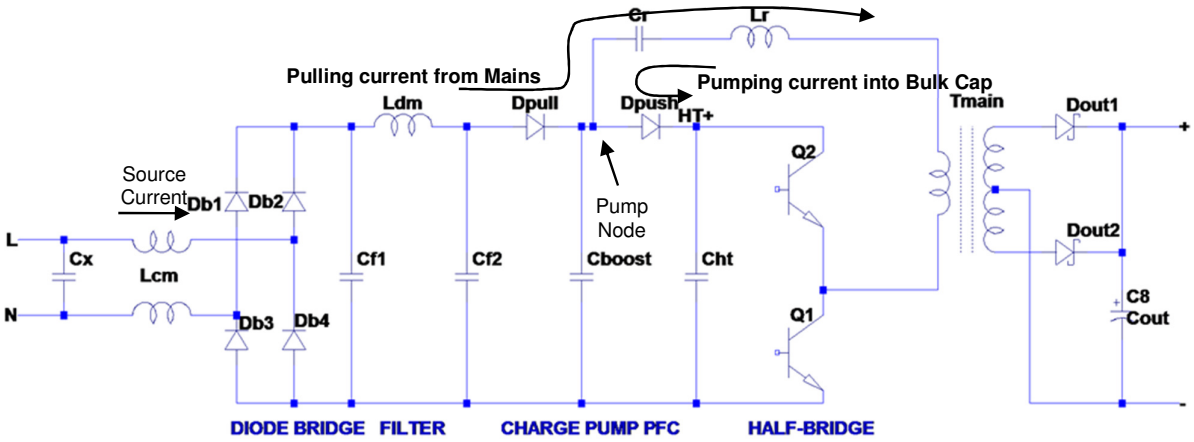

Figure 3: Charge Pump PFC (simplified schematic)

A typical design has the power factor and harmonic emissions optimised for nominal line and load. The value of **C_{BOOST}** is typically chosen so that the voltage swing on the pump node is just enough to ensure charge pumping occurs at all points in the mains cycle. The important waveforms are shown in Figure 4.

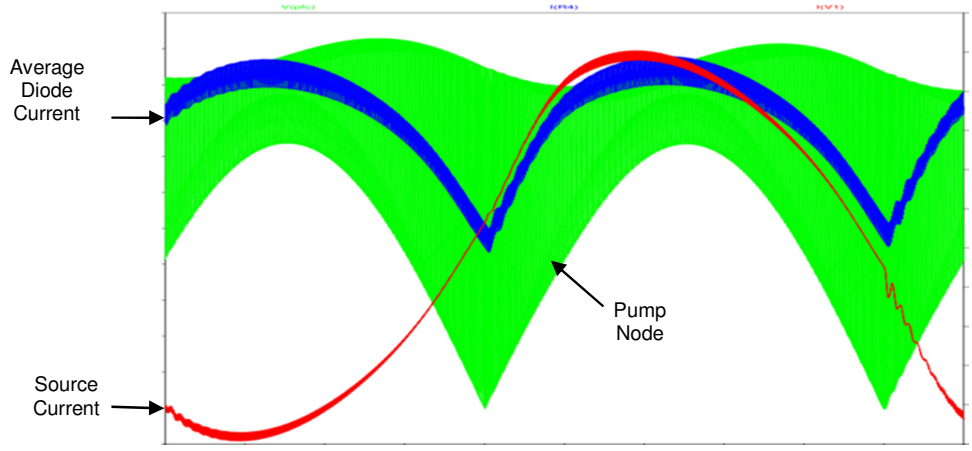

Figure 4: Charge Pump PFC Waveforms (at nominal line, load)

However, at the line/load extremes, the power factor and harmonic emissions are worse. At high line and low load, the voltage swing on the pump node is not enough to achieve charge pumping when the line voltage is crossing through zero, so that the line current has flat portions on each side of the zero crossing, see Figure 5. Conversely, at low line and high load, the voltage swing on the pump node is too large, which causes steep edges on the line current waveform around the zero crossing point.

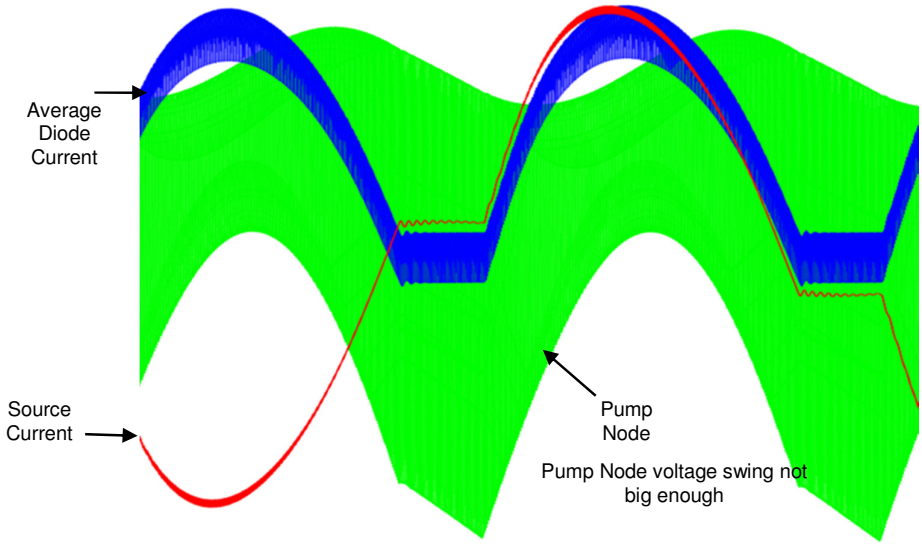

Figure 5: Pump Node waveforms (max line, min load)

The achievable power factor and harmonics emissions performance depends on the range of line and load conditions that the application has to handle. The charge pumping arrangement described above is usually good enough for lower power applications, but some higher power applications require an additional charge pump to be incorporated, as shown in Figure 6.

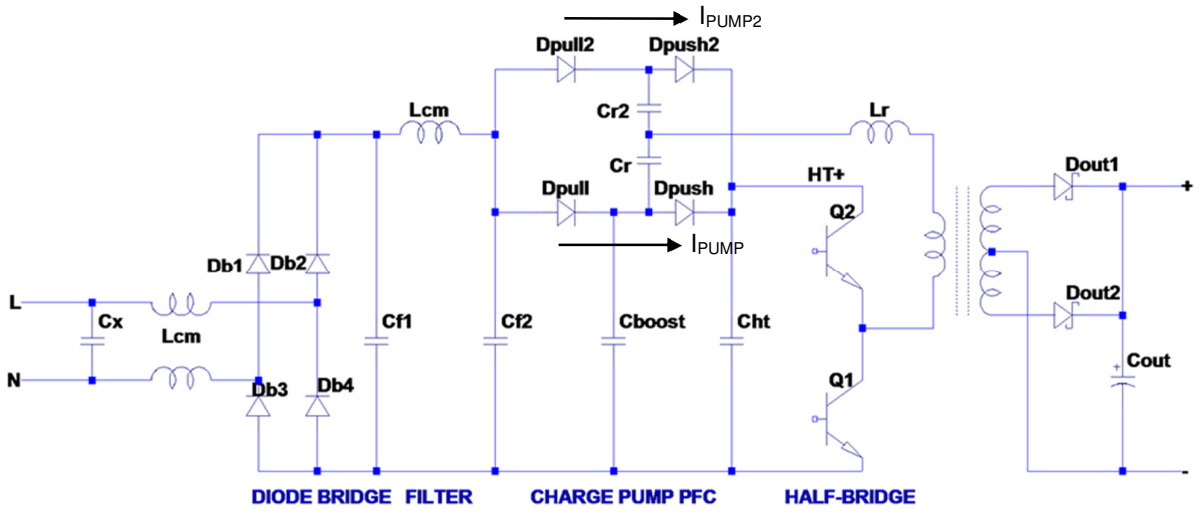

Figure 6: Dual Charge Pump PFC (simplified schematic)

As before, $\mathbf{C_{BOOST}}$ is the boost control capacitor influencing the amount of boosting provided by the first charge pump stage. However, the second (smaller) charge pump stage ($\mathbf{D_{PULL2}}$, $\mathbf{D_{PUSH2}}$ and $\mathbf{C_{R2}}$) does not have a boost capacitor and so it pumps charge across almost the entire line cycle, as shown by the waveforms in Figure 7. Because the two charge pumps have different characteristics, the current pumped by each stage has a different shape. When added together, the combined current waveform shows better power factor and lower harmonic content at the line/load extremes than that achieved by the single charge pump PFC.

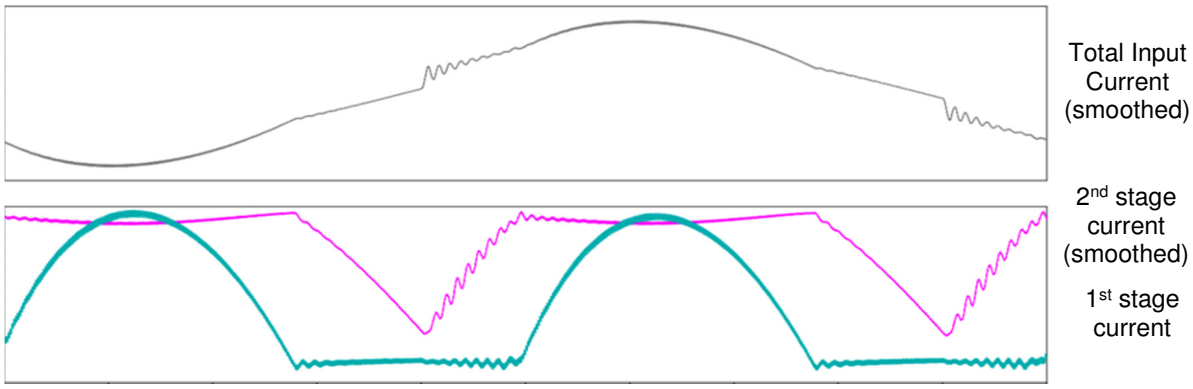

Figure 7: Line shaping with two Charge Pump PFC stages

Actual Charge Pump Arrangements

The simplified circuits shown in Figure 3 and Figure 6 are given as equivalent schematics to help with understanding how it works. In Figure 8, the schematic is slightly different, because the controller IC (with current sense resistor R_{CS}) must be referenced to the negative rail.

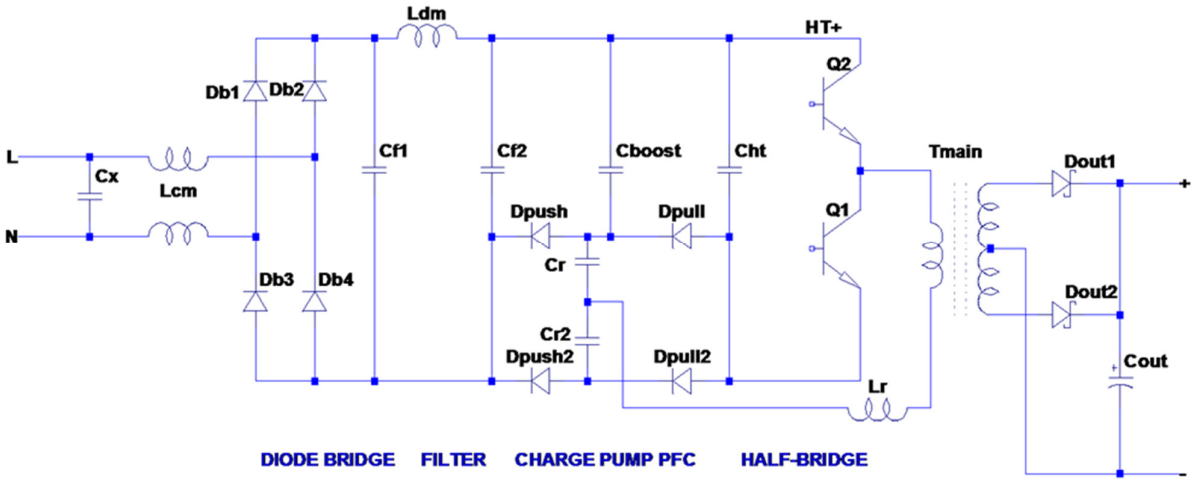

Figure 8: Inverted dual charge pump (simplified schematic)

Here the charge pumping has been moved to the negative side between the COM and HT- rails; this is because the GND connection of the controller IC needs to be referenced to one end of the current sensing resistor. The charge pumping diodes (D_{PUSH}, D_{PUSH2}, D_{PULL}, D_{PULL2}) need to be fast recovery types. The bridge diodes can be standard recovery types.

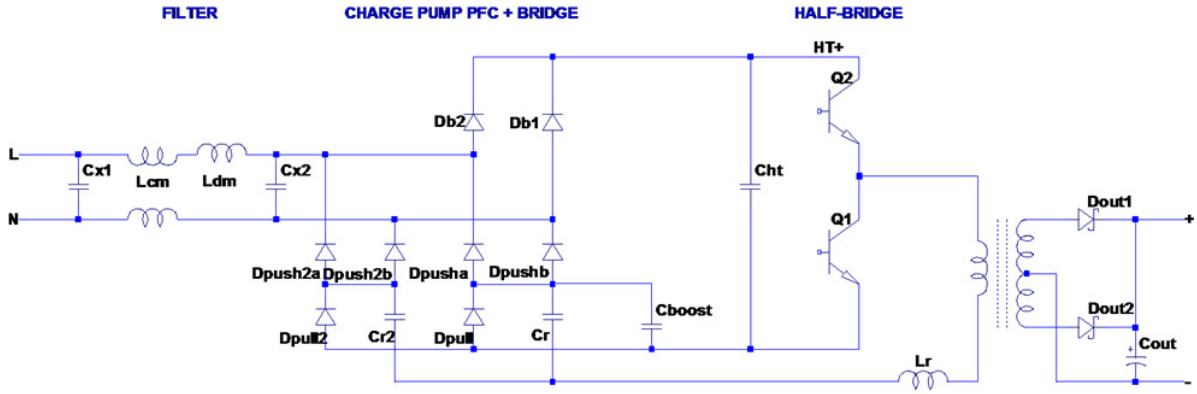

Figure 9: Combined Dual Charge Pump PFC and Bridge

With the arrangement in Figure 8, there are four diodes in the current path between the line inputs, An alternative arrangement is given in Figure 9, which achieves the same thing but has only three diodes in the primary current path. This reduces the total forward diode conduction losses, making this arrangement preferred for applications which are efficiency-critical. The switching diodes should be fast recovery types such as FR105 to minimise losses.

Detailed Design Notes RED2501

The schematic of a typical 40W LED Driver design is shown for reference in Figure *10*.

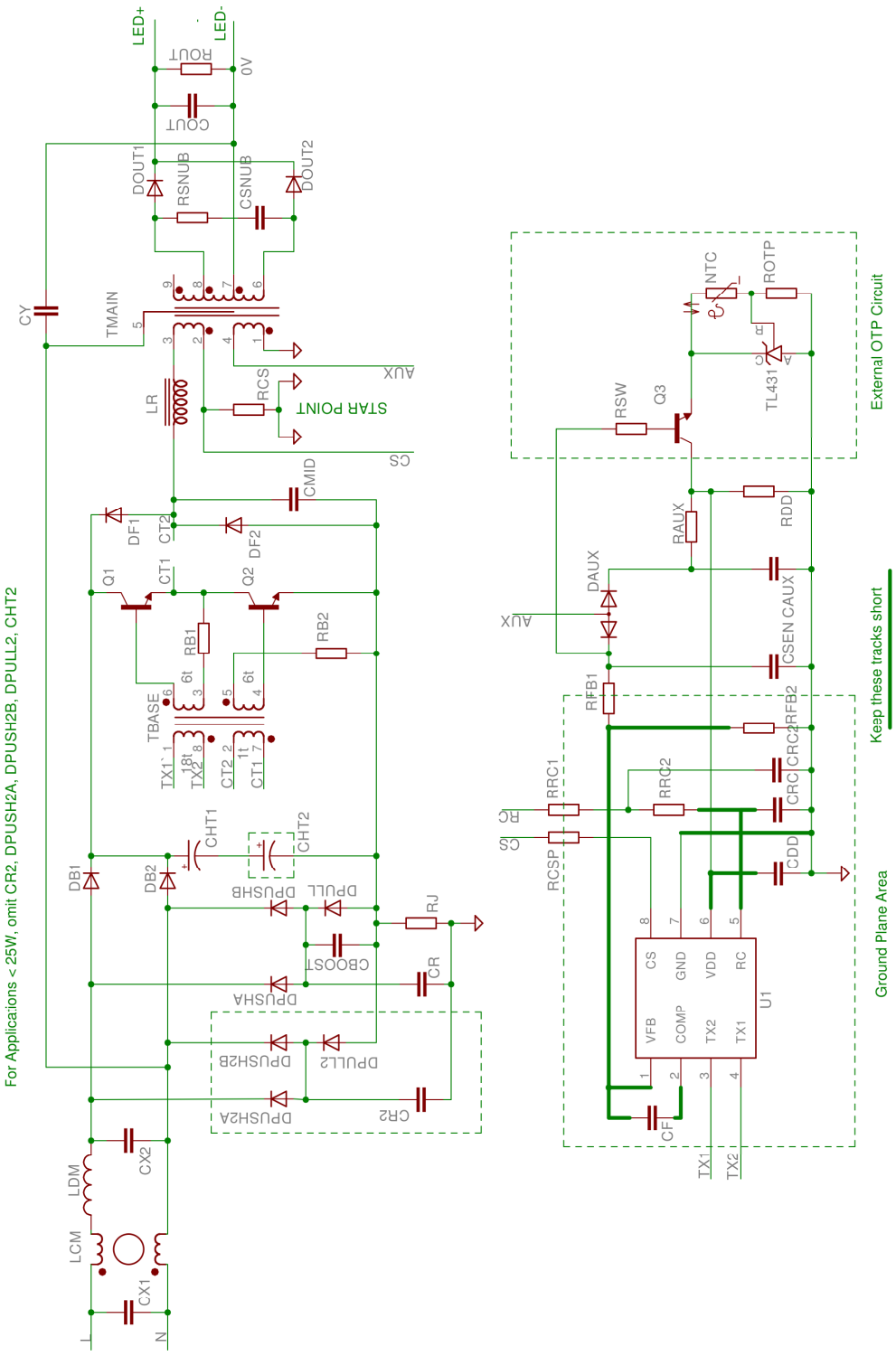

Figure 10*: 40W LED Driver Schematic using RED2501*

Controller

The sub-schematic for other control IC blocks are shown in the following schematics.

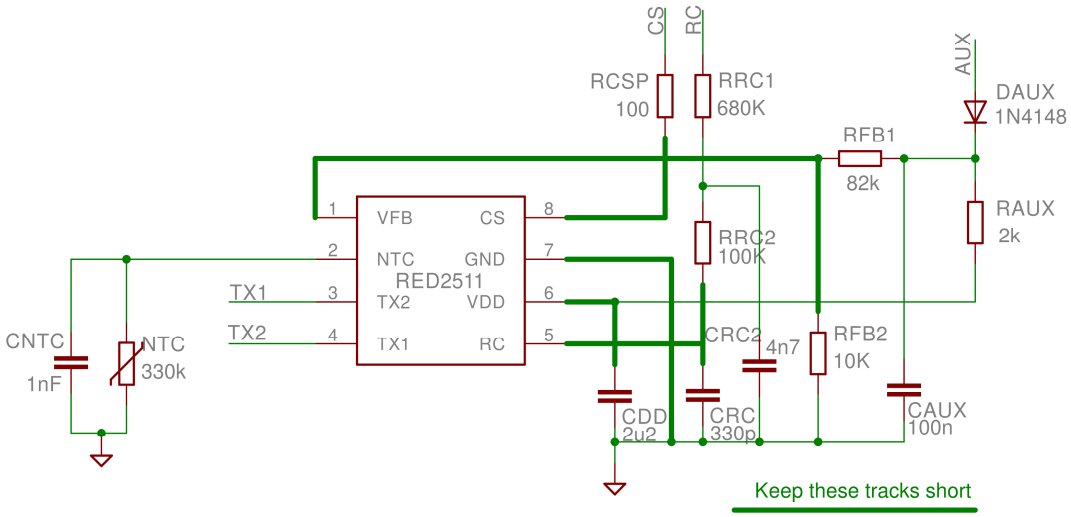

Figure 11: RED2511 Controller block schematic

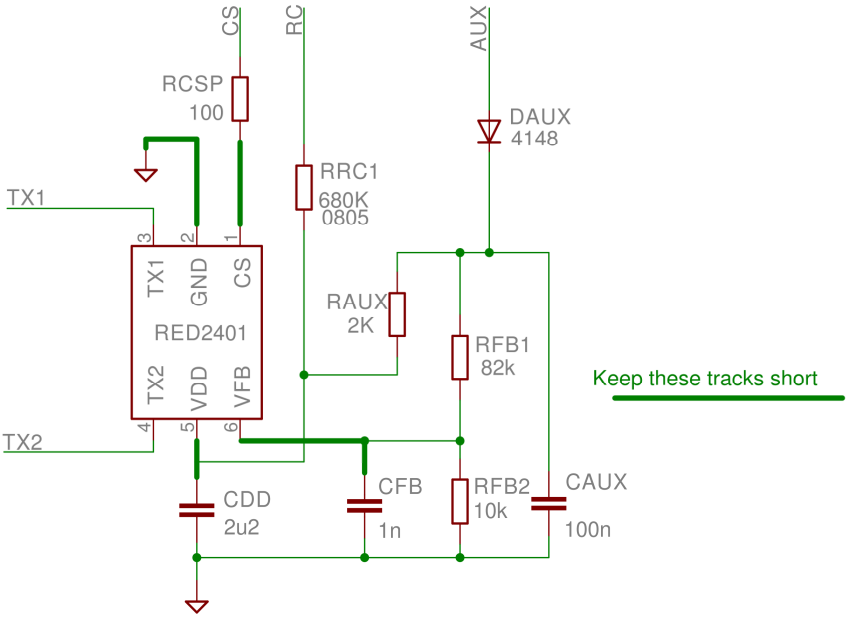

Figure 12: RED2401 Controller block schematic

Supply Rails

The control IC's incorporate a low power shunt regulator, which normally maintains the V_{DD} supply rail at V_{DDREG} [3.45V] and requires I_{DDRUN} [700uA]. The controller IC will shut down if the VDD supply drops below V_{UVD}. The value of R_{AUX} is determined by the equations below:

$$V_{AUX(MIN)} = (V_{OUT(MIN)} \times N_A/N_S - V_{DIODE}) \text{ V}$$
$$V_{UVD(MAX)} = V_{DDREG(MAX)} - \Delta V_{DDSLEEP} \text{ V}$$
$$R_{AUX} < (V_{AUX(MIN)} - V_{UVD(MAX)})/I_{DDRUN(MAX)} \ \Omega$$

Example
For a 40W 230Vac application, assuming:

$V_{OUT(MIN)} = 25$ V
$N_A = 5$ turns
$N_S = 19$ turns
$V_{DIODE} = 0.6$ V
$V_{DDREG(MAX)} = 3.6$ V (from datasheet)
$\Delta V_{DDSLEEP} = 0.45$ V (from datasheet)
$I_{DDRUN(MAX)} = 800$ uA (from datasheet)

$V_{AUX(MIN)} = 25V \times \frac{5t}{19t} - 0.6V = 5.98$ V
$V_{UVD(MAX)} = 3.6V - 0.45V = 3.15$ V
$R_{AUX} < \frac{5.98V - 3.15V}{800u} = 3.54k \ \Omega$
Therefore, choose $R_{AUX} = 2k \ \Omega$

The value of C_{DD} is sized big enough to hold up the VDD supply rail during start up, and is typically 2.2uF.

Timing Components

The preferred values for R_{RC2}, C_{RC} and C_{RC2} are:

R_{RC2} = 100k
C_{RC} = 330p
C_{RC2} = 1n

The value for R_{RC1} determines the oscillator frequency range, calculated from the equation below:

$$R_{RC1} = 2M46 \times 60k/F \times V_{IN}/230 \ \Omega$$

As well as controlling the oscillator frequency, R_{RC1} also provides the current for starting up the controller, together with R_J. The time taken to start up is given by the equation below:

$$t_{STARTUP} \cong (C_{DD} + C_{AUX}) * V_{DDSTART}/(\frac{V_{IN} \times \sqrt{2}}{(R_{RC1} + R_{RC2} + R_J)} - I_{DDSLEEP} - \frac{V_{DDSTART} + V_{UVD}}{2 \times R_{DD}}) \text{ seconds}$$

Example
Calculate the maximum (worst case) start up time.
If the application requires:

R_{RC1} = 2M46Ω
R_{RC2} = 100kΩ
R_J = 2M46Ω
C_{DD} = 2.2uF
C_{AUX} = 100nF
R_{DD} = ∞ (not fitted)

$V_{IN(MIN)}$ = 198V
$I_{DDSLEEP(MAX)}$ = 12uA
$V_{DDSTART(MAX)}$ = 4.0V

$$t_{STARTUP} \cong (2.2u + 100n) * 4V / \left(\frac{198V \times \sqrt{2}}{(2M46+100k+2M46)} - 12u - 0\right) = 209ms$$

Current Sensing

The primary current is sensed by the CS pin, which is connected to the current sensing resistor R_{CS} via padding resistor R_{CSP} (typically 100Ω). R_{CSP} is used to prevent damage to the IC during surge conditions. It has no other purpose.
The value of the current sense resistor R_{CS} is given by the equation below:

$$R_{CS} = 0.27 \times \frac{40W}{P_{NOM}} \times \frac{V_{IN}}{230V} \text{ Ohms}$$

Example
If the application requires:

P_{NOM} = 25 W
V_{IN} = 115V

Calculate current sense resistor:

$$R_{CS} = 0.27 \times \frac{40W}{25W} \times \frac{115V}{230V} = 0.216 \text{ Ohms}$$

Voltage Sensing

The output voltage is sensed by the VFB pin, to protect the output against over-voltage when unloaded.
The values of the voltage control loop components are given below:

R_{FB1} = 47 kΩ
$R_{FB1} = R_{FB2} \times (V_{AUX(MAX)} - V_{REF})/V_{REF}$

where

$$V_{AUX(MAX)} = V_{OUT(MAX)} \times N_A/N_S - V_{DIODE}$$

Example
For a typical 40W application assume:

$V_{OUT(MAX)}$=45V
N_A=5t
N_S=19t
V_{REF}=1.2V (from datasheet)
R_{FB2} = 10 kΩ

$$V_{AUX(MAX)} = 45 \times \frac{5}{19} - 0.6 = 11.2V$$

$$R_{FB1} = 10k \times \frac{11.2-1.2V}{1.2V} \cong 82k$$

Protection Features

Capacitive Mode Protection

CSOC converters are not able to operate in capacitive mode. The base drive transformer (in conjunction with the IC) will prevent the converter operating in capacitive mode. Good designs will ensure that the converter does not enter capacitive mode in normal operation. If the base drive inductance is not enough, the transistors can turn off prematurely. If this occurs, the capacitive mode protection feature in the IC will become active and the base drive transformer will effectively set the converter operating frequency.

Open Circuit Protection (OCP)

At light load or no load condition, the rectified primary side auxiliary voltage will be increased. If the VFB pin voltage rises to 1.2V (the internal reference voltage) the chip enters CV mode instead of CC mode, regulating the output voltage by varying the switching frequency.

Feedback Protection (FBP)

If voltage feedback loop is broken, the IC shuts down and performs a fault recovery sequence (see below).

Short circuit protection (SCP)

When output terminals are short circuited, the IC detects an abnormally low voltage on the VFB pin. The IC shuts down and performs a fault recovery sequence (see below).

Over Temperature Protection (OTP)

IC has an internal over temperature shutdown level (see datasheet for details of OTP trip point). The IC shuts down and performs a fault recovery sequence (see below).

Fault Recovery Sequence

After a fault is detected, the controller shuts down and performs 7 dummy reboot cycles and attempts to reboot on the 8th cycle. The controller repeats this sequence until the fault condition has been removed. The timing for each reboot cycle is determined by the timing resistor R_{RC} + R_{RC1} and the combined value of decoupling capacitance on the VDD and AUX supply rails. The reboot time can be calculated by the formula below:

$$t_{REBOOT} \cong 8 \times (C_{DD} + C_{AUX}) * \frac{(V_{DDSTART} - V_{UVD})}{\frac{V_{IN}}{R_{RC}+R_{RC2}+R_J} - I_{DDSLEEP} - \frac{V_{DDSTART}+V_{UVD}}{2 \times R_{DD}}} \text{ secs}$$

Example

Calculate the typical fault recovery time.

If the application requires:

R_{RC1} = 2M46Ω
R_{RC2} = 100kΩ
R_J = 2M46Ω
C_{DD} = 2.2uF
C_{AUX} = 100n
R_{DD} = not fitted

V_{IN} = 230V
$I_{DDSLEEP}$ = 8uA
$V_{DDSTART}$ = 3.6V
V_{UVD} = 3.0V

$$t_{STARTUP} \cong 8 \times (2.2u + 100n) * (3.6V - 3.0V) / \left(\frac{230V \times \sqrt{2}}{(2.46M + 100k + 2.46M)} - 8u - 0\right) = 195ms$$

Additional protection

The IC can be shut down by an external circuit. There are three suggested methods for this:

1) Pull the VFB pin to > V_{REF} [1.2V]: IC shuts down and performs a fault recovery sequence (see below).
2) Pull down the VDD pin to < V_{UVD} [3.0V]: IC shuts down, restarts when VDD pin is released.

An example of an external over-temperature protection circuit (using the second method) is shown in Figure *10*.

Bridge and Charge Pumps

Boost capacitor C_{BOOST}

The boost capacitor is sized by scaling from reference designs.
For single charge pump PFC applications (Power <25W):

$$C_{BOOST}(target) = 10 \times \frac{P_{OUT}}{20} \times \frac{230V}{V_{IN}} \times \frac{40}{F} \text{ nF}$$

For dual charge pump PFC applications (Power >25W):

$$C_{BOOST}(target) = 15 \times \frac{P_{OUT}}{40} \times \frac{230V}{V_{IN}} \times \frac{60}{F} \text{ nF}$$

Example
For a 30W 115Vac application, assuming:

$F_{TAR} = 50$ kHz (target average frequency) then

$$C_{BOOST}(target) = 15 \times \frac{30}{40} \times \frac{230V}{115} \times \frac{60}{50} = 27 \text{ nF}$$

$$C_{BOOST}(actual) = \mathbf{27} \text{ nF}$$

Resonant Components

The resonant components are calculated by scaling from reference designs.
First, calculate the capacitor scaling factor Kc:

$$K_C = \frac{P_{NOM}}{40} \times \frac{60k}{F_{TAR}} \times [\frac{230}{V_{IN}}]^2$$

Where

P_{NOM} = Nominal output power (W)
F_{TAR} = target average frequency at nominal line and load (kHz)
V_{IN} = Nominal line voltage (V_{RMS})

Now calculate the target values for the resonant capacitors as follows:

For High Power Designs (P_{NOM}>25W):

$$C_R(target) = 27 \times K_C \text{ nF}$$
$$C_R(target) = 12 \times K_C \text{ nF}$$

For Low Power Designs (P_{NOM}<25W):

$$C_R(target) = 44 \times K_C \text{ nF}$$

Choose the nearest available values for each capacitor.
Estimate the actual average frequency, based on the actual capacitor values chosen:

For High Power Designs (P_{NOM}>25W):

$$F_{ACT} = F_{TAR} \times \frac{C_{R2}(target)+C_R(target)}{C_{R2}(actual)+C_R(actual)} \text{ kHz}$$

For Low Power Designs (P_{NOM}<25W):

$$F_{ACT} = F_{TAR} \times \frac{C_R(target)}{C_R(actual)} \text{ kHz}$$

The inductance value L_R should be chosen as per the following equation:

$$L_R = 1 \times \frac{40}{P_{NOM}} \times \frac{60}{F_{ACT}} \times [\frac{V_{IN}}{230}]^2 \text{ mH}$$

Example

Application requires a single stage charge pump PFC:

P_{NOM} = 20 W
F_{TAR} = 40 kHz
V_{IN} = 115V

Calculate capacitor scaling factor:

$$K_C = \frac{P_{NOM}}{40W} \times \frac{60k}{F_{TAR}} \times [\frac{230V}{V_{IN}}]^2 = 3$$

Calculate target capacitor values:

$$C_R(target) = 22 \times 3 = 66 \text{ nF}$$

Choose actual capacitor values:

$$C_R(actual) = 68 \text{ nF}$$

Estimate actual minimum frequency:

$$F_{ACT} = F_{TAR} \times \frac{66}{68} = 38.8 \text{ kHz}$$

Calculate resonant inductor value:

$$L_R = \frac{40W}{20W} \times \frac{60k}{38.8k} \times [\frac{V_{IN}}{230V}]^2 = 0.75\text{mH}$$

Half-Bridge Block

For detailed information on RediSem's CSOC and transistor drive technology, please consult AN2113. This document explains the circuit operation and component requirements for RediSem's patented half-bridge arrangement.

Base drive Transformer (T_{BASE})

RediSem's designs are based on CSOC (Controlled Self-Oscillating Converter) technology. This means that it is like a self-oscillating design where the IC is in control of the frequency which regulates the output. Very importantly, the base drive transformer does not control the frequency of the converter, the IC does. The base drive transformer is only necessary to provide power to the transistors. Changing the number of turns or core material will not affect driver's operating power, but it will affect transistor temperature and operating performance at extreme temperatures and line/load combinations. Please be cautious when changing anything relating to the base drive transformer. Base drive transformer may be procured fully assembled and tested from Acme Electronics (越丰电子（广州）有限公司). For further details, please see AN2113.

Transistor choice (Q1, Q2)

Transistor choice is important in RediSem's LED driver solutions. Please begin by using transistors that RediSem recommends. When selecting other transistors, choose transistors with low fall time (t_f) and low storage times (t_s). Also, do not use transistors that are too big as larger transistors typically have higher switching losses. RediSem typically chooses transistors with a continuous collector current rating that is 2-3 times higher than the peak current the transistor sees in normal operation.

Base Resistors

The base resistor values affect the transistor storage and fall times. Choose large base resistor values to achieve fast turn-off times. However, make sure that the reflected drive voltage appearing on the Tx pins of the controller IC does not exceed the datasheet limits (4V).
As a starting point, choose the value for the base resistors from the following equation:

$$R_{B1} = R_{B2} = \frac{40W}{P_{OUT}} \times \frac{V_{IN}}{230V}\ \Omega$$

Flywheel Diodes

D_{F1} and D_{F2} provide a route for the primary magnetizing current to return to the HT+ and HT- supply rails. The types chosen should be fast turn on and fast recovery to ensure snap-free commutation. (Note that most datasheets do not specify turn-on time). If these diodes have too slow turn-on, it can cause switching transistors Q1, Q2 to run hot, due to shoot-through current spikes. Good diode types are HS1J available from Taiwan Semi (台湾半导体有限公司).

Mid-point capacitor (C_{MID})

There is a mid-point capacitor on the half-bridge output which helps to reduce switching losses in the transistors and suppress RF emissions. The capacitor should be rated for 4x nominal line voltage. As a starting point, use the following equation:

$$C_{MID} = 680 \times \frac{40W}{P_{OUT}} \times \frac{V_{IN}}{230V}\ \text{pF}$$

Main Transformer

[Please also refer to AN2112: "LLC Transformer design for EMI"]

Transformer Calculations

The desired transformer turns ratios are given by the following equations:

$$V_{PRI(MAX)} < \frac{VOUT(MIN)}{VOUT(MAX)} \times \frac{V_{IN(MIN)}^2}{198\times\sqrt{2}} \text{ V}$$

$$\frac{N_P}{N_S} = \frac{V_{PRI(MAX)}}{V_{OUT(MAX)}}$$

$$\frac{N_A}{N_S} > (V_{UVD(MAX)} + V_{DIODE} + 2k \times I_{DDRUN(MAX)})/V_{OUT(MIN)}$$

Example
Calculate turns ratio Np/Ns:

Application requirements:
- $V_{OUT(MIN)}$ = 25V
- $V_{OUT(MIN)}$ = 45V
- $V_{IN(MIN)}$ = 198VAC
- $V_{IN(MAX)}$ = 264VAC

$$V_{PRI(MAX)} < \frac{25}{45} \times \frac{198^2}{198\times\sqrt{2}} = 78 \text{ V}$$

So, choose $V_{PRI(MAX)}$ =76V.
Then

$$\frac{N_P}{N_S} = \frac{76}{45} = 1.69$$

Transformer Structure

The recommended transformer design is shown in the figures below. A screen layer is added between primary winding and secondary winding. The screen winding should be correctly connected to a quiet point of the primary circuit. This arrangement can cancel out most of the common mode noise, minimising conducted RF emissions.

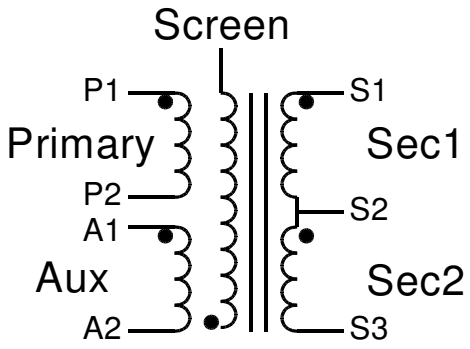

Figure 13: Transformer Schematic

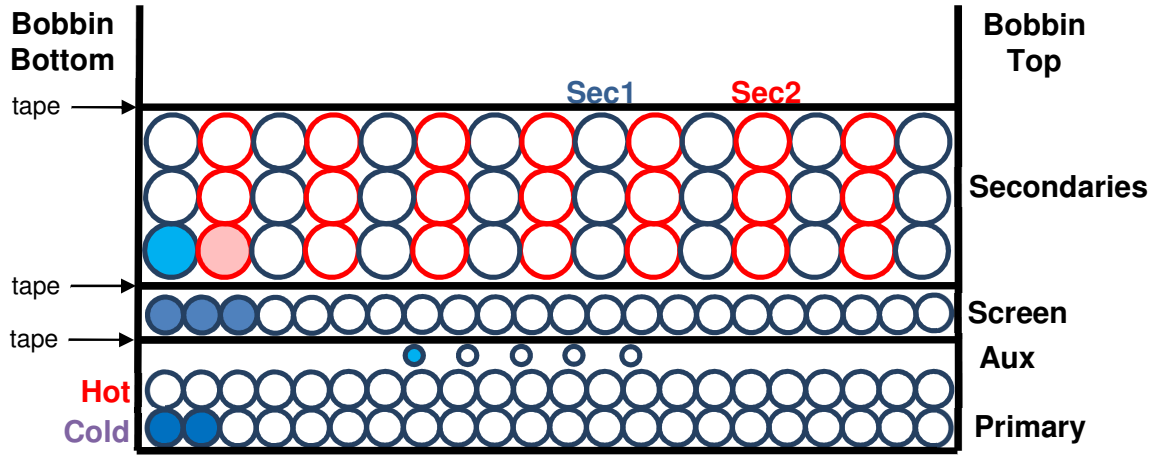

Figure 14: Typical Transformer Winding Arrangement

Bulk Capacitor

For a demanding application such as high power factor (P_{OUT}>25W) and wide output voltage range (50-100%), the peak voltage appearing on the bulk capacitor **C_{HT}** can reach as much as 150% of peak line voltage under worst case conditions (high line, low load). In this case, it is usually best to use two identical capacitors in series (C_{HT1}, C_{HT2}) to achieve the necessary voltage rating at low cost.

However, If the power factor target can be reduced (e.g. P_{OUT}<25W) or the output range reduced (e.g. 70-100%) then the peak HT voltage can be reduced enough to allow a single 450V capacitor to be used.

Output Rectification

The output diodes are chosen to have adequate voltage and current rating with low conduction and switching losses.

The value of output capacitance affects the peak output voltage when the output is open-circuited while operating. The minimum output capacitance is therefore given by the following equation:

$$C_{OUT} > 150 \times \frac{P_{OUT}}{40W} \times \frac{(V_{SELV}^2 - 50^2)}{V_{SELV}^2 - V_{OUT(MAX)}^2} \text{ uF}$$

Example
Calculate minimum value of output capacitance:

Application requirements:
P_{OUT} = 20W
V_{SELV} = 60V
$V_{OUT(MAX)}$ = 40V

$$C_{OUT} > 150 \times \frac{20W}{40W} \times \frac{(60^2 - 50^2)}{60^2 - 40^2} = 41 \text{ uF}$$

Line Input Protection

For overcurrent protection, a conventional fuse is recommended, with adequate current rating and slow rupture characteristics to withstand High Energy Surge tests. Alternatively, a 2R2 fuse resistor may be used, but this will reduce the overall efficiency and increase the internal case temperature.

Additional protection against line Over-Voltage conditions, such as High Energy Surges, is normally not required, as the design already has line filtering directly on the line input. Additionally, the half-bridge topology used here has plenty of voltage headroom on the switching devices (unlike typical flyback designs).

Inrush current limiting is provided by the inherent resistance of the line filter block, in particularly the common-mode choke.

Surge components

RediSem solutions use a half-bridge configuration with 700V transistors (V_{CES}). This means that the transistors can survive with an HT bus voltage of up to 700V. Passing a 500V or 1kV differential surge requirement therefore means keeping the HT bus below 700V during a surge, or below 650V to have some margin. The HT capacitor combined with the input impedance (resistance of the fuse-resistor as well as CM and DM chokes) is usually enough to resist the surge, but an MOV can also be added if the input impedance is small.

Be very careful during surge testing and use proper safety precautions.

EMI Measures

Line Filtering

Conducted RF Emissions are suppressed by a differential-mode choke, a common-mode choke and two class-X capacitors. Note that if the class-X capacitors are made too large, the Power Factor will be reduced.

Snubber

A secondary snubber can improve RF emissions in the range 5-15MHz.

Y-Capacitor

It should not be necessary to use a class “Y” capacitor across the isolation barrier if care is taken when designing the transformer. Ensure that the secondary windings are adequately screened from the primary circuit.

PCB Layout

Ground Star Point

The CS pin is sensitive to noise injected from surrounding components and tracks. Treat the COM end of R_{CS} resistor as the COM star point between the controller block and the power circuit, to avoid noise induced by switching current loops (see Figure 10). Keep the track length from the CS pin to R_{CSP} resistor as short as possible. Do not pass the main load current underneath the IC.

Keep the Aux power loop small. The loop from the Aux winding, passing through D_{AUX}, C_{AUX} and returning to the transformer winding should be short. The GND return from C_{AUX} does not have to be connected back to the star point.

High voltage nodes

Be careful to minimise track lengths of high voltage nodes and keep these well away from the control IC. If using a drum core for the resonant inductor (L_R), note that the hot end (i.e. the end connected to Q1, Q2) can couple noise into the control IC. Also keep the drum core apart from any magnetic EMI components to avoid EMI problems due to unwanted magnetic coupling.

Sensitive Nodes

Tracking of sensitive circuit nodes, particularly pins VFB, RC and CS of the controller IC should be protected by a ground plane and distanced well away from hot nodes, such as the switching BJTs and the resonant inductor. These tracks should be kept short, as noted in the example schematic in Figure 10.

Keep R_{RC2} close to the IC, minimising the track length and area of the RC pin.

V_{DD} decoupling capacitor

Keep the power tracks to the decoupling capacitor C_{DD} very short.

Troubleshooting

Note: when attaching probes to the board under test, use a large common-mode choke in the line input to avoid getting misleading results and waveforms, and even damaging the circuit under test. Best to use COM (pin 7 of the controller IC) as the scope ground reference point.

Start-up

Controller not starting

Check TX1, TX2 pins on IC for drive pulses with peaks >2V. If no signal activity here, possible faults include:

D_{AUX} damaged, wrong way round
R_{DD} value too low
C_{DD} leaky, wrong polarity
IC damaged

BJTs not commutating

Check the Mid-Point node for large voltage waveforms (Vpkpk > 200V). If absent, possible faults include:

T_{BASE} windings incorrect
R_{B1}, R_{B2} damaged
Q_1, Q_2 damaged
CS pin open-circuit
C_{MID} too big
Open-circuit fault in primary current loop
IC damaged

No output

With output disconnected and line input off, measure the output terminals for sign of short-circuit. If none, possible faults include:

Output diodes, capacitor
Secondary windings phasing incorrect

Turns on, but turns off after a short while (1-5ms)

Check VDD and primary current during start up. If VDD falls to the $V_{DDSLEEP}$ level during the start-up, then increase CDD and/or decrease COUT. Possible errors are:

C_{DD} too small
Current limit error
T_{MAIN} aux winding too few turns
R_{AUX} value too large
C_{DD}, C_{AUX}, R_{AUX}, or D_{AUX} faulty/missing

Regulation

Current Limit Error

Value of R_{CS}
T_{MAIN} turns ratio

Poor Current regulation

Check current waveform for any sharp peak waveforms that occur during an entire mains cycle. Check for excessive noise on the VFB pin by putting a 10nF capacitor from VFB to GND. Other items to check:

R_{CS} temperature coefficient and tracking around R_{CS}
T_{MAIN} saturation
L_R saturation
T_{MAIN} primary inductance too low
R_{RC1} or C_{RC} wrong value (frequency limiting)
T_{BASE} inductance too low
PFC/boosting fault
Capacitive Mode switching (at minimum line, maximum load)
Noise coupling into VFB or CS pin

LED Flashes

Check for T_{MAIN} Saturation
Reduce the number of LED's and re-check
Check the voltage on the VFB pin, it should be less than 1.2V under normal operation
Check VDD is above 3V

Strange current waveforms

Sometimes it may be possible to see missing commutations, where a regular current waveform suddenly jumps. This is usually caused by interference on one of the IC's sensitive pins. Check to see if the problem reduces when a 10nF capacitor is fitted between the VFB and GND pins. Also try reducing the size of R_{CSP} to 10R. Add a 1uF capacitor directly to the VDD and GND pins of the IC.

If these fixes cure the problem, then a proper fix should be found. Move the sensitive nodes away from the "hot" nodes, such as the midpoint switched node. Also make sure that the tracks connecting the Vdd capacitor, RC components and Vfb components are not far away from the IC.

Hot Transistors

Conduction Losses

Using a voltage clamped scope probe amplifier (or equivalent) measure the on-state voltage. Check that the on-state voltage of both transistors is <300mV. If the on-state is higher than this, possible causes include:

Transistor current rating or h_{FE} too small
Base drive transformer turns ratio too large

Switching Losses

Check the storage and fall times of both transistors using scope probes to monitor the base-emitter and collector-emitter waveforms. At minimum line voltage and maximum load, the storage time (t_{STOR}) should be roughly 200ns and the fall time (t_F) should be <200ns. If this is not the case, possible causes include:

Transistors too slow
R_{B1}, R_{B2} values too small
T_{BASE} inductance too high
C_{MID} too small

Shoot-through

Monitor the collector current of Q1 (or Q2) using a current transformer. If there are any sharp current spikes in the waveform, please check:

Base Drive transformer windings
Flywheel diodes turn-on too slow
C_{MID} wrong side of T_{BASE} primary winding

Adding a 10nF ceramic capacitor between base and emitter of Q1 and Q2 can help to supress shoot-through.

EMI

Conducted Emissions

50k – 500kHz
Differential-mode:
Increase C_{X1}, C_{X2} and L_{DM} (Note: as C_{X1} increase, PF reduces)

Common-mode:
Make sure that the screen direction is correct. Also, adjust screen winding turns
Increase L_{CM} or the Y-Capacitor
Check PCB tracking. Make sure that the noisy midpoint node is not close to the secondary or mains input.

2MHz – 30MHz
Secondary snubber
T_{BASE} PCB tracking

Radiated Emissions

30 - 100MHz
Check the tracking on around the base drive transformer. Too long wires or too much
Test to see if one of the diodes is causing ringing. Add 100pF across D_{AUX} and 1nF across the output diodes. If the noise reduces in frequency, then you need to find an appropriate snubber for the
Divide the midpoint capacitor C_{MID} into two and place directly across the freewheel diodes DF1 and DF2

Harmonics Emissions

Non-compliant at low line, high load

Boost voltage too high
C_{BOOST} value too small
C_R, C_{R2} values too large

Non-compliant at high line, low load

Boost voltage too low
C_{BOOST} value too large
C_R, C_{R2} values too small

Power Factor

As for Harmonics Emissions above, plus:
C_{X1}, C_{X2} values too large

Fault Protection

Open-circuit Voltage too high

Voltage control loop unstable
C_{SEN} too large
R_{FB1}, R_{FB2}, C_{FB} values incorrect

Commutation unstable
C_{MID} too large
T_{BASE} inductance too large

Capacitive Mode Operation

Switching (at minimum line, maximum load)
L_R, C_R, C_{R2}, C_{BOOST} values incorrect
T_{MAIN} turns ratio too low

Fault Recovery Time

Too short
Increase C_{DD}, R_{RC1} (adjust C_{RC} to keep same clock setting)
Decrease R_{DD}

Too long:
Decrease C_{DD}, R_{RC1} (adjust C_{RC} to keep same clock setting)
Increase R_{DD}

About RediSem

RediSem designs and supplies semiconductor ICs for energy efficient power management applications. RediSem uniquely combines extensive experience in power electronics with in-depth knowledge of IC design and manufacturing and works with the world's top suppliers and customers. RediSem's unique patented IC and converter technologies deliver maximum efficiency and performance, while reducing overall bill of materials cost through the use of bipolar transistors.

RediSem's range of LED control ICs can be used with RediSem's patented single stage LED control solution to provide very high efficiencies with low EMI – all with a single IC. When combined, these features deliver a low cost, high performance LED driver solution.

RediSem's fluorescent driver controller ICs achieve the advanced performance of MOSFET drivers by using bipolar transistors at a fraction of the BOM cost. RediSem's range of SMPS (Switched Mode Power Supply) control ICs enables low-cost LLC converters with bipolar transistors that deliver very high efficiencies already meeting DoE Level VI regulations, have low standby power and have much lower EMI compared to flyback converters.

All RediSem ICs are supported by comprehensive turn-key application designs enabling rapid time to market. For further information please use our contact details below

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