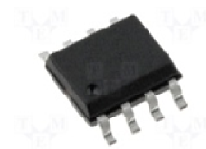
RED2201

Fluorescent Ballast Control IC

Features

- Advanced digital controller IC for bipolar transistor ballasts
- Closed loop current control
- Adjustable preheat time
- Controlled ignition ramp
- Capacitive mode detection
- Automatic dead-time control
- Lamp removal detection
- Lamp fault protection
- End-Of-Life detection
- Auto-restart after fault
- Micro-power operating current (<1mA)



SO-8N

Applications

- Fluorescent ballasts
- Single or Multiple lamp configurations
- Passive or Active PFC ballasts

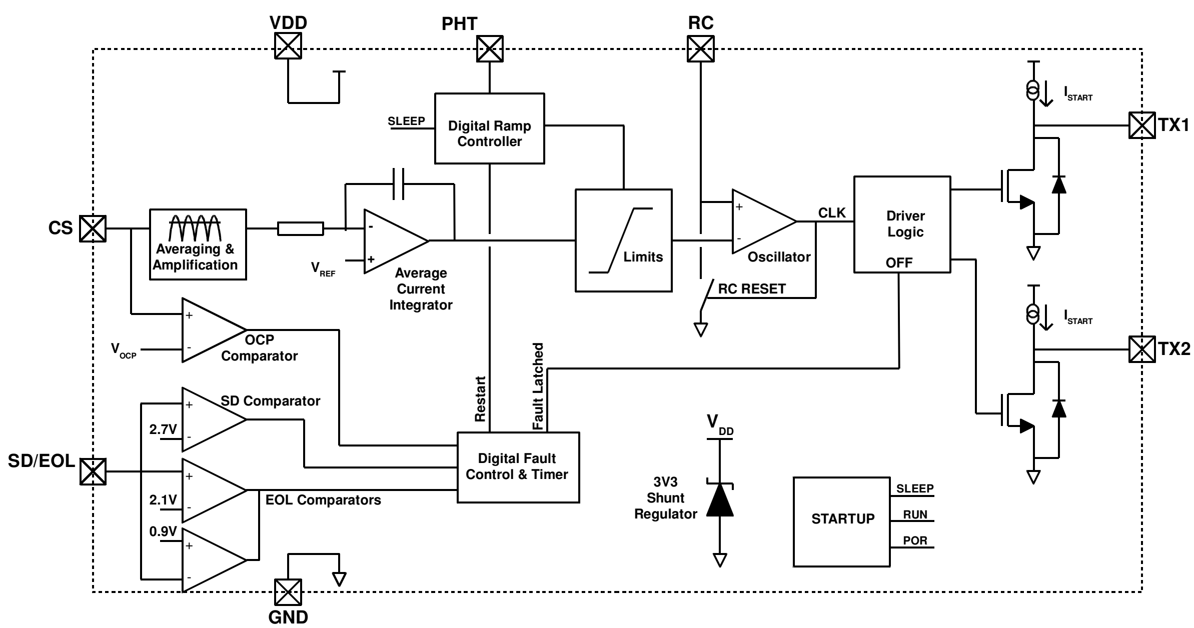


Figure 1: Block Diagram

Device Pins

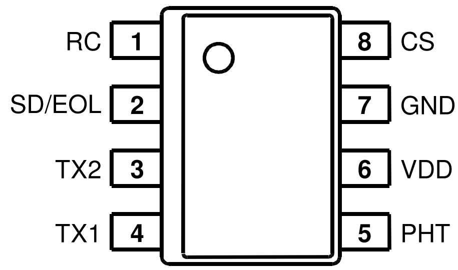


Figure 2: SO-8N pin connections (top view)

Pin Functions

Pin #	Name	Function
1	RC	External RC network sets the minimum switching frequency. 30k, 330p = 40kHz
2	SD/EOL	Shutdown and End-Of-Life detection. Shutdown when V_{SD}>2.7V. EOL when 0.9V > V_{SD}> 2.1V
3	TX2	Output to base drive transformer
4	TX1	Output to base drive transformer
5	PHT	Program pin for preheat time
6	VDD	This pin provides power to the IC. Connect a 470nF capacitor between VDD and GND (pin 7)
7	GND	Chip ground
8	CS	Current sense input for preheat current control and protection features

Typical Application

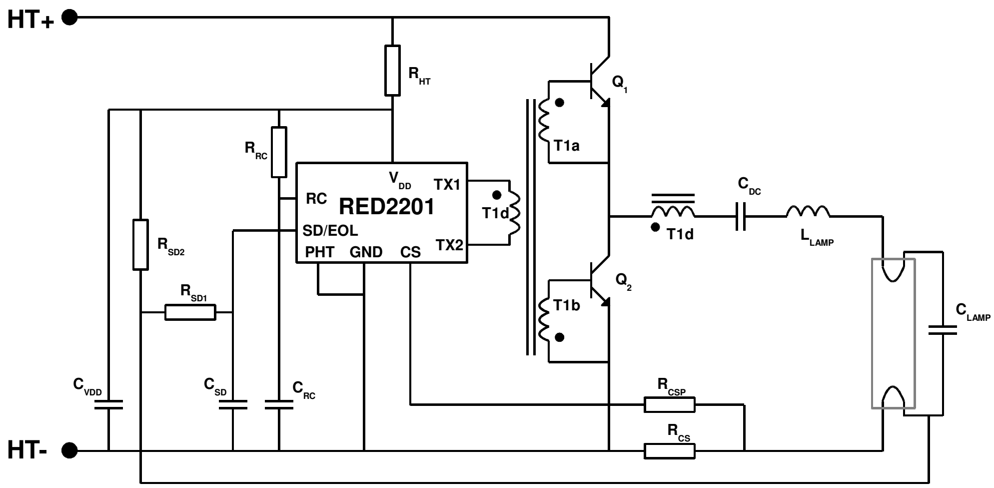


Figure 3: RED2201 Application diagram

Application Overview

The RED2201 is a controller IC specific for fluorescent lighting ballasts. It enables the use of low-cost robust bipolar transistors lamps as switching devices through patented CSOC (Controlled Self-Oscillating Converter) topology. The lamp operating modes (start, preheat, ignition, run) are all controlled by the IC. The average ballast current is controlled by modulating the operating frequency. Preheat time is programmable through the PHT pin and the designer can set the operating frequencies using the RC pin. Internal over-current protection (OCP) and a versatile Shutdown and End-Of-Life pin (SD/EOL) enable protection against lamp faults, after which RED2201 will automatically restart when the faulty lamp has been replaced.

CSOC base drive technology

RED2201 uses patented CSOC (Controlled Self Oscillating Converter) technology to drive bipolar transistors in a standard half-bridge series LC converter used for fluorescent lamps. This type of ballast circuit uses robust low cost bipolar transistors along with a simple base drive transformer that provides the bulk of the base drive to turn the transistors on. The converter naturally self-commutates and the IC used to force the end of each commutation cycle to control the frequency.

Robust technology

CSOC drive technology allows robust and low-cost bipolar transistors to be used instead of expensive MOSFETs. For a 35W T5 ballast small TO92 13003 transistor types are sufficient. CSOC technology does not suffer from many of the problems associated with MOSFET ballasts, such as dead-time, capacitive switching and limited over-current capability.

Dead_time control

One of the benefits of CSOC technology is that dead-time control is automatic. In MOSFET based ballasts it is essential to ensure that the dead-time is controlled accurately otherwise it can lead to damage in the MOSFETs. In a RED2201 ballast, dead-time is optimally controlled within the IC. CSOC technology ensures that the transistors can never hard switch which greatly simplifies the design process.

Capacitive mode Protection

A another CSOC benefit is that capacitive mode switching cannot occur. In MOSFET based ballasts capacitive mode switching can quickly lead to damage of the transistors, for example when the lamp fails to strike or when the lamp is removed.

In a RED2201 ballast, the ballast is prevented from entering capacitive mode. Before the ballast enters capacitive switching, the ballast frequency is increased so that capacitive switching cannot occur. This means that failure to strike and lamp removal will not result in transistor damage.

RED2201 Operation

RED2201 provides a complete ballast solution, including all the features necessary to control a long-life lamp ballast with protection and re-start features. The IC includes:

- Controlled start ramp which allows the ballast components to initialise
- Controlled preheat current to optimise the filament heating
- Controlled ignition ramp
- Fixed ballast frequency in burn mode
- Fault detection circuitry
- Re-start when lamp has been replaced

A flow chart showing the ballast operation is shown in Figure 4.

Figure 3 shows a typical Ballast application for the RED2201 IC and figure 6 shows the typical ballast switching frequency, lamp current and lamp voltage profiles, which are all controlled by the RED2201 IC.

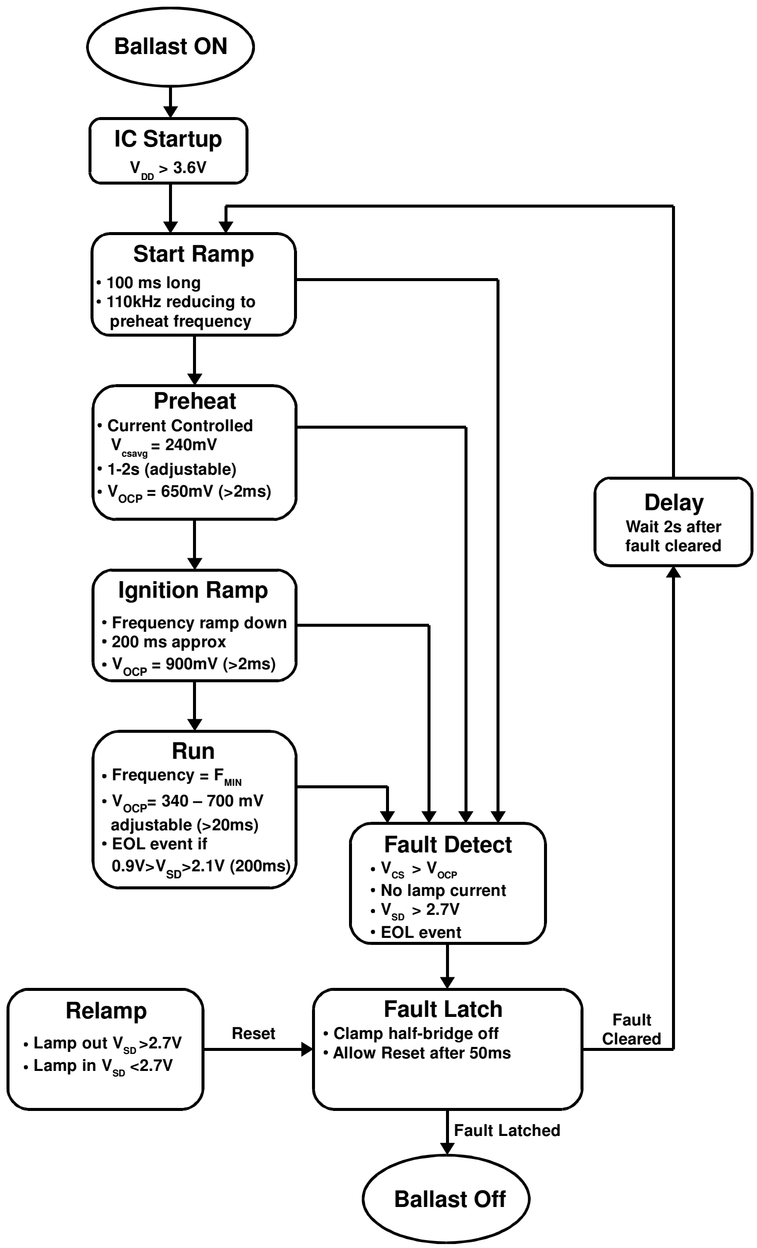


Figure 4: RED2201 Operation Flow Chart

IC Startup

The startup and operating current of the RED2201 is supplied through R_{hv}. Figure 5 shows typical waveforms for the RES2201 IC at startup. In SLEEP mode the IC and transistors are off and an I_{DD} of 0.5mA ($I_{DDSLEEP}$) is required to pull the V_{DD} pin voltage up to 3.6V ($V_{DDSTART}$). The IC then starts and a controlled zener clamp inside the IC regulates the V_{DD} voltage down to 3.3V (V_{DDREG}). The IC operating current is nominally 0.5mA (I_{DDRUN}) plus any excess current that is required to clamp V_{DD} to 3.3V. If power is removed from the ballast and V_{DD} falls below 2.7V ($V_{DDSLEEP}$), the IC enters SLEEP mode and will only restart if sufficient $I_{DDSLEEP}$ is supplied to reach $V_{DDSTART}$.

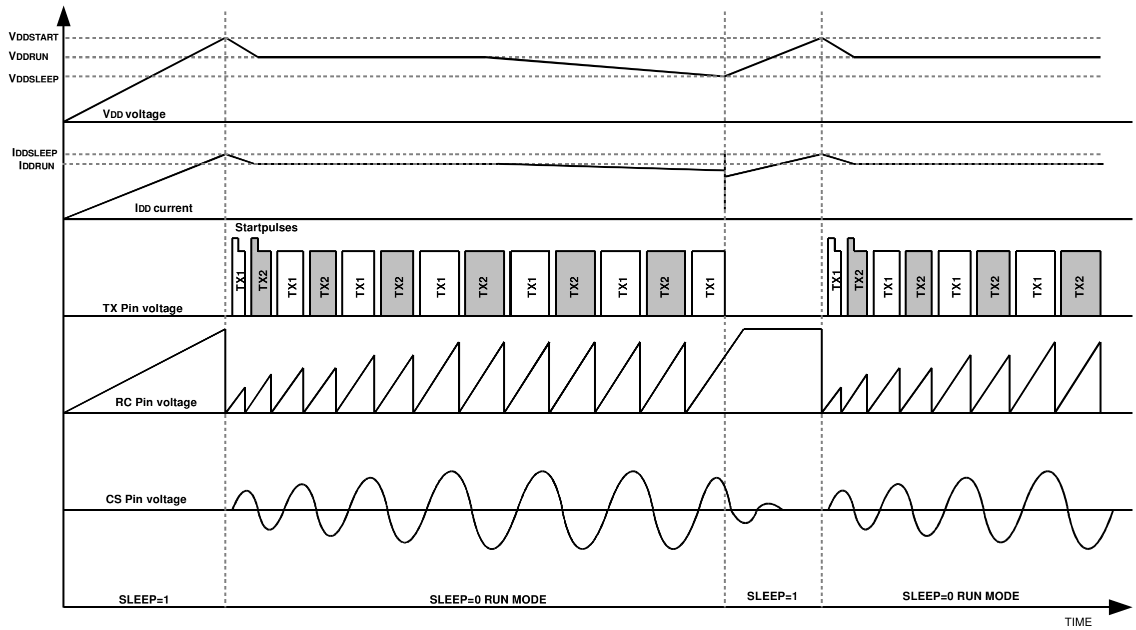


Figure 5: RED2201 Startup waveforms

Start Ramp

When RED2201 turns on it issues start current pulses via the base drive transformer T1 to switch the bipolar transistors Q1 & Q2 on and off. The initial operating frequency of the ballast (FSTART) is high (about 110kHz) to allow time for the series resonant tank components to settle down. In Start mode the switching frequency is ramped down for approximately 50ms until the average voltage on the CS pin reaches its control value V_{CSPH} (200mV).

If during start mode the operating frequency is too high for the resonant components and the oscillations stop, the IC will again try to re-start the oscillations by re-issuing start pulses. During this time the frequency is continually reduced along the start ramp.

Preheat

At the end of the start-ramp RED2201 goes into Preheat mode and controls the lamp current. Preheat current is controlled by varying the switching frequency. The IC senses the voltage at the CS pin and adjusts the half-bridge frequency to control the average current. The current control circuit is entire inside the IC, the only components required to set the preheat and run currents are resistors R_{cs}. The following equation gives an initial approximation for R_{cs}.

$$R_{CS} = \frac{0.3}{I_{PH}}$$

Where I_{PH} is the required RMS preheat current of the lamp. R_{cs} will typically vary from 1 Ω for a small lamp down to 0.2 Ω for two large lamps.

The current averaging circuit, control loop and compensation components are all internal to RED2201. The preheat time is set inside RED2201 by a timer that counts the number of oscillator cycles from IC start-up. When the preheat timer overflows the Ignition mode is started.

Three different preheat timer values can be programmed through the PHT (Pre-Heat Time) pin giving typical preheat times of 1s, 1.5s and

2.0s. Short PHT to GND to enable 2s preheat; short PHT to V_{DD} to enable 1.5s preheat; or provide $V_{DD}/2$ to PHT to enable 1s preheat time.

Ignition

At the beginning of the ignition ramp frequency is slowly reduced at a fixed rate, which increases the voltage across the lamp. When the voltage across the lamp is sufficiently high it is ignited and starts to burn. The switching frequency continues ramping down to a minimum frequency.

Run

Once F_{MIN} is reached RED2201 is in Run mode. The minimal operating frequency of the ballast is programmed by C_{RC} and R_{RC} connected to the RC oscillator pin. The run frequency F_{MIN} can be calculated as follows:

$$F_{MIN} = \frac{1}{(2.4 \times R_{RC} \times C_{RC} + 0.8us)}$$

The resonant tank components L_{lamp} and C_{lamp} need to be chosen appropriately to ensure the correct lamp voltage in preheat and run modes. It is recommended that a 330pF, 5% COG capacitor is used for C_{RC}. For 40 kHz operation choose R_{RC} to be 30 kΩ.

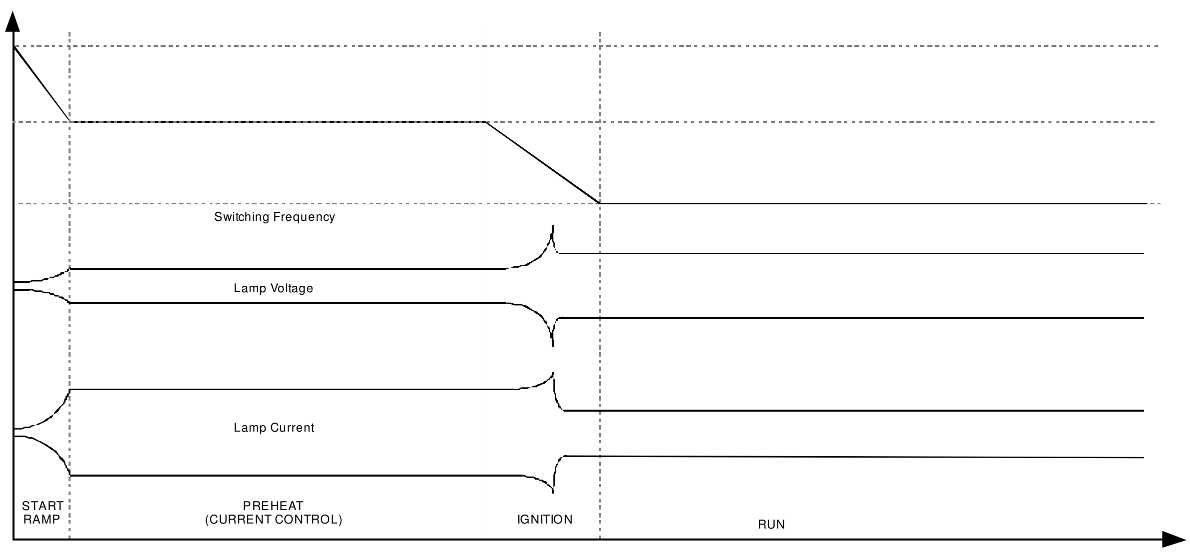


Figure 6: Ballast operating modes with RED2201

Ballast Protection features

RED2201 is able to detect a variety of lamp faults through its CS and SD pins. To ensure faults are real they will need to be triggered for a number of switching cycles. If a fault remains for a certain period, then the ballast is latched off safely. The ballast is allowed to re-start only when a lamp has been replaced or the power is recycled. A schematic of the ballast protection circuit is shown in figure 7 below.

Table 1 gives a summary of common faults conditions in an RED2201 ballast system.

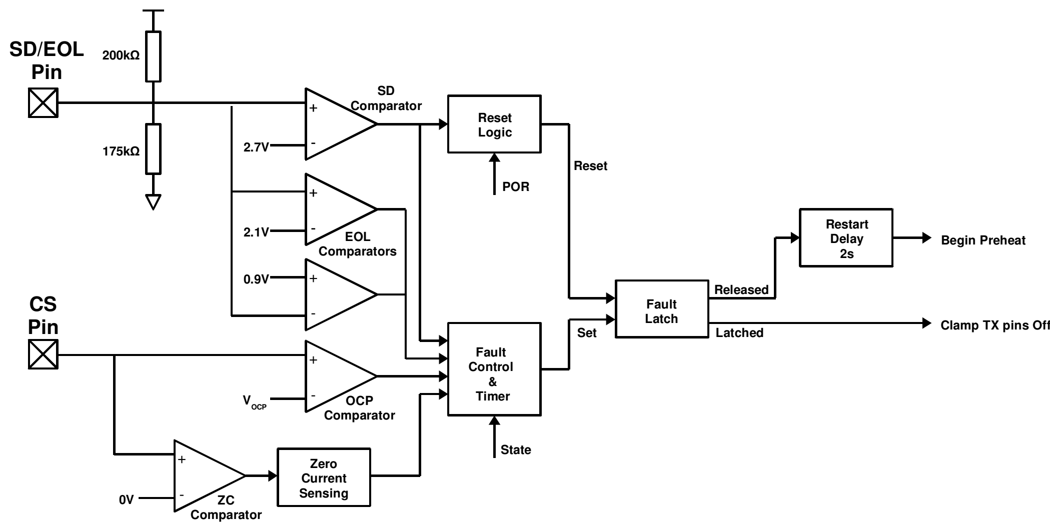


Figure 7: Fault protection circuit inside RED2201

SD/EOL pin

RED2201's SD/EOL pin allows the user to configure a variety of different fault conditions.

A 0.9-2.1V window comparator is used to detect asymmetric lamp voltages when a lamp reaches End-Of-Life. The EOL detection is only enabled in RUN mode and an EOL fault is triggered if the EOL condition exists for more than 200ms.

A fault is also triggered if during any time the SD/EOL pin voltage exceeds 2.7V.

Once the IC's fault latch has been triggered it can be reset when a re-lamp event is detected at the SD/EOL pin. A re-lamp is defined as the SD voltage moving over and then below 2.7V. This can be easily achieved through detection resistors connected to the lamp filaments. The SD pin has 200kΩ resistors to both GND and VDD to simplify the SD circuit design.

No-Current

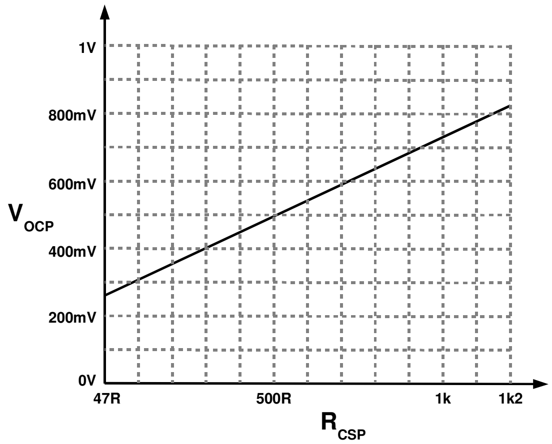
Unlike a MOSFET converter, the CSOC converter stops oscillating if there is no lamp current. So, if a lamp is removed, its filaments have failed or opened, the half-bridge stops switching. When the CS pin senses that there are no zero crossings (i.e. no lamp current) the IC will trigger a fault condition.

Overcurrent

The IC also protects against over-current thorough the CS pin. If the instantaneous peak CS pin voltages exceed V_{OCP} the IC will trigger a fault condition. The trigger value V_{OCP} has three separate levels for preheat, ignition and run. The value of VOCP is 650mV in preheat and 900mV during ignition. In Run mode the VOCP level is adjusted with RCSP, which is calculated using the equation:

$$R_{CSP} = 3.2 \times (V_{OCP} - 340)$$

where V_{OCP} is the desired over-current threshold in Run mode expressed in mV. The following equation shows the value of R_{CSP} for a typical range of V_{OCP} values. The value of R_{CSP} should not normally be outside the range of 47Ω to 1 kΩ.



Fault delay time

When a fault is triggered it is necessary to make sure that the fault is real, so RED2201 features a fault time-out. During preheat and ignition the fault time-out is set to approximately 2ms and during run it is set to approximately 20ms (EOL fault >200ms). If a fault has remained beyond this period, the IC latches the fault and clamps the TX pins low, thus stopping the half-bridge.

Auto-Restart

The IC then latches the ballast off and waits for the lamp to be removed and re-inserted before it tries to re-start. It senses >2.7V on the SD pin (through R_{SD1} and R_{SD2}) when a lamp has been removed because the filament resistance no-longer pulls the SD pin below its 2.7V threshold. When a new lamp is re-inserted, the SD pin is again pulled below 2.7V and the fault condition in the IC is cleared and the ballast is allowed to re-start.

After lamp re-insertion the IC waits for approximately 2 seconds before starting the ballast again. When the ballast re-starts it goes through the normal start ramp, preheat, ignition and run modes. If the fault remains, the ballast will again detect the fault and latch off, waiting for the lamp to be removed and replaced.

Capacitive mode Protection

Through the CS pin, the IC can sense when the ballast is about to enter into capacitive mode. If the CS pin detects an early zero-crossing of the ballast current the switching cycle is immediately terminated and the half-bridge is commutated by changing the state if the TX pins.

Issue	State & time-out			Condition	IC Behaviour	Protection	Resolution
	PH	IGN	RUN				
No Lamp	√ 2ms	√ 2ms	√ 20ms	*No current in ballast circuit*	*No zero crossing detected at CS pin*	*Latch fault Shut down*	*Restart on re-lamp or V_{dd} recycle*
Short circuit on any lamp terminal	√ 2ms	√ 2ms	√ 20ms	*High peak currents*	*OCP detected at CS pin*	*Latch fault Shut down*	*Restart on re-lamp or V_{dd} recycle*
Diode test (de-activated lamp)	√ 2ms	√ 2ms	√ 20ms	*High peak current at ignition due to inductor saturation*	*OCP detected at CS pin*	*Latch fault Shut down*	*Restart on re-lamp or V_{dd} recycle*
End-Of-Life			√ 200ms	*Asymmetric lamp currents*	*SD/EOL pin voltage outside window >200ms*	*Latch fault Shut down*	*Restart on re-lamp or V_{dd} recycle*
Mains overvoltage			√ 20ms	*High ballast currents*	*OCP detected at CS pin. Trigger Level adjustable.*	*Latch fault Shut down*	*Restart on re-lamp or V_{dd} recycle*
Inductor saturation on ignition		√ 2ms		*Very high peak currents and hard-switching*	*IC adjusts frequency and keeps switching if event <2ms*	*If >2ms Latch fault and Shut down*	*Restart on re-lamp or V_{dd} recycle*
Capacitive Mode operation			√	*Hard-switching causes increased losses and limits power delivered to lamp*	*IC immediately detects hard-switching at CS and TX pins*	*IC increases operating frequency*	*Frequency increased until no hard-switching detected*

Table 1: Summary of Faults in an RED2201 ballast system

PCB Design Guidelines

Vdd decoupling capacitor

RED2201 is a very low power IC. It consumes just over 1mW. It also has to provide large currents to start the converter. It can therefore be sensitive to noise on its supply. It is therefore recommended to use a 470nF decoupling capacitor connected between the V_{DD} and GND pins of the IC. When designing the PCB, keep the power tracks to the decoupling capacitor short. It is particularly important to keep the GND track as short as possible.

CS track

The CS pin is sensitive to noise injected from surrounding components and tracks. Small capacitive coupling from a high voltage source to the CS pin can lead to problems with the sensing circuits inside the IC. It is therefore important to keep the track length from the CS pin to R_{CSP} as short as possible.

RC tracking

To maximise efficiency the timing capacitor should be kept small. It is recommended that a 330pF capacitor is used to provide a good compromise between efficiency and stability. The track that joins the RC pin, R_{RC} and C_{RC} should be kept as short as possible. There should not be any high voltage nodes close to it. The connection between CRC and the GND pin of the IC should also be kept as short as possible.

High Voltage Nodes

High voltage switching nodes, such as the midpoint of the half-bridge should be kept away from the IC pins. All the nodes between the half-bridge switching point and the top side of the lamp are considered to be sensitive nodes. To avoid problems with injected noise any sensitive track can be shielded using GND tracking around the sensitive node.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Permanent damage may result if a device is subjected to operating conditions at or in excess of absolute maximum ratings.

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	V_{DD}		-0.5	4.0	V
Supply current	I_{DD}		-10	10	mA
Pin Input/output voltage	V_{IO}		-0.5	V_{DD} + 0.5	V
Pin Input/output current	I_{IO}		-10	10	mA
Junction temperature	T_J		-25	125	℃
Storage temperature	T_P		-40	125	℃
Lead temperature	T_L	Soldering, 10 s		260	℃

NORMAL OPERATING CONDITIONS

Unless otherwise stated, electrical characteristics are defined over the range of normal operating conditions. Functionality and performance is not defined when a device is subjected to conditions outside this range and device reliability may be compromised.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply current	I_{DD}	V_{DD} shuntreg off (V_{DD} < V_{DDREG})	0.5		0.7	mA
Full-Power (minimum) switching frequency	F_{NOM}	R_{RC} = 30k; C_{RC}=330p		40		kHz
Junction temperature	T_J			25		℃

ELECTRICAL CHARACTERISTICS

Unless otherwise stated:

- Min and Max electrical characteristics apply over normal operating conditions.
- Typical electrical characteristics apply at $T_J = T_{J(TYP)}$ and $I_{DD} = I_{DDREG(TYP)}$.
- The chip is operating in RUN mode.
- Voltages are specified relative to the GND pin.

VDD Pin

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DDRUN}	To enter RUN mode	3.2	3.6	4.0	V
	V_{DDREG}	In RUN mode	3.1	3.3	3.5	V
	$\Delta V_{DDSLEEP}$	To enter SLEEP mode (measured relative to V_{DDREG})		-600		mV
Supply current	I_{DDREG}	In RUN mode, $V_{DD} < V_{DDREG}$	0.5		0.8	mA
	$I_{DDSLEEP}$	In SLEEP mode	0.3		0.8	mA

SD/EOL Pin

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SD fault threshold voltage	V_{SD_FAULT}	DC voltage at SD pin	2.4	2.7	3.0	V
SD Fault delay time – Preheat & Ignition	T_{FD_SD}	Assuming 55 kHz operating frequency	3		5	ms
SD Fault delay time – Run	T_{FD_SD}	Assuming 40 kHz run frequency	15		20	ms
Restart delay time	T_{RD}	Assuming 40 kHz run frequency, PHT to V_{DD}		2		s
EOL max threshold	V_{SD_EOL+}	EOL enabled in RUN only	1.9	2.1	2.3	V
EOL min threshold	V_{SD_EOL-}	EOL enabled in RUN only	0.8	0.9	1.0	V
EOL fault delay time	T_{FD_EOL}	EOL enabled in RUN only		200		ms

CS Pin

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Average current regulation threshold voltage - preheat	V_{CSPH}	70kHz square-wave	240	265	290	mV
Overcurrent threshold (OCP) Preheat	V_{OCPPH}	Preheat	550	650	700	mV
Overcurrent threshold (OCP) Ignition	V_{OCPIGN}	Ignition	800	900	1000	mV
Overcurrent threshold OCP Run	V_{OVPRUN}	Adjusted with R_{CSP} resistor	340		700	mV
OCP Fault delay time – preheat & ignition	T_{FD_OCP}	Assuming 55 kHz operating frequency. PHT connected to Vdd	2		4	ms
OCP Fault delay time – run	T_{FD_OCP}	Assuming 40 kHz run frequency. PHT connected to Vdd	20		40	ms

RC Pin

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Start Frequency	F_{START}	C_{RC}=330pF, R_{RC}=30kΩ	100	110	120	kHz
Start Frequency down ramp	dF/dt_{start}	C_{RC}=330pF, R_{RC}=30kΩ		0.2		kHz/ms
Start ramp time	T_{ST}	C_{RC}=330pF, R_{RC}=30kΩ, f_{PH}=55kHz		100		ms
Ignition Frequency down ramp	dF/dt_{ign}	C_{RC}=330pF, R_{RC}=30kΩ		0.1		kHz/ms
Run Frequency	F_{RUN}	C_{RC}=330pF, R_{RC}=30kΩ .	37	40	44	kHz
Preheat Frequency Range	F_{PHX}	C_{RC}=330pF, R_{RC}=30kΩ .	37		120	kHz

PHT Pin

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Short preheat time	T_{PHTS}	PHT connected to 1/2 Vdd F_{pre} = 65kHz		1.0		s
Medium preheat time	T_{PHTM}	PHT shorted to V_{DD} , F_{pre} = 65kHz		1.5		s
Long preheat time	T_{PHTL}	PHT shorted to GND , F_{pre} = 65kHz		2.0		s

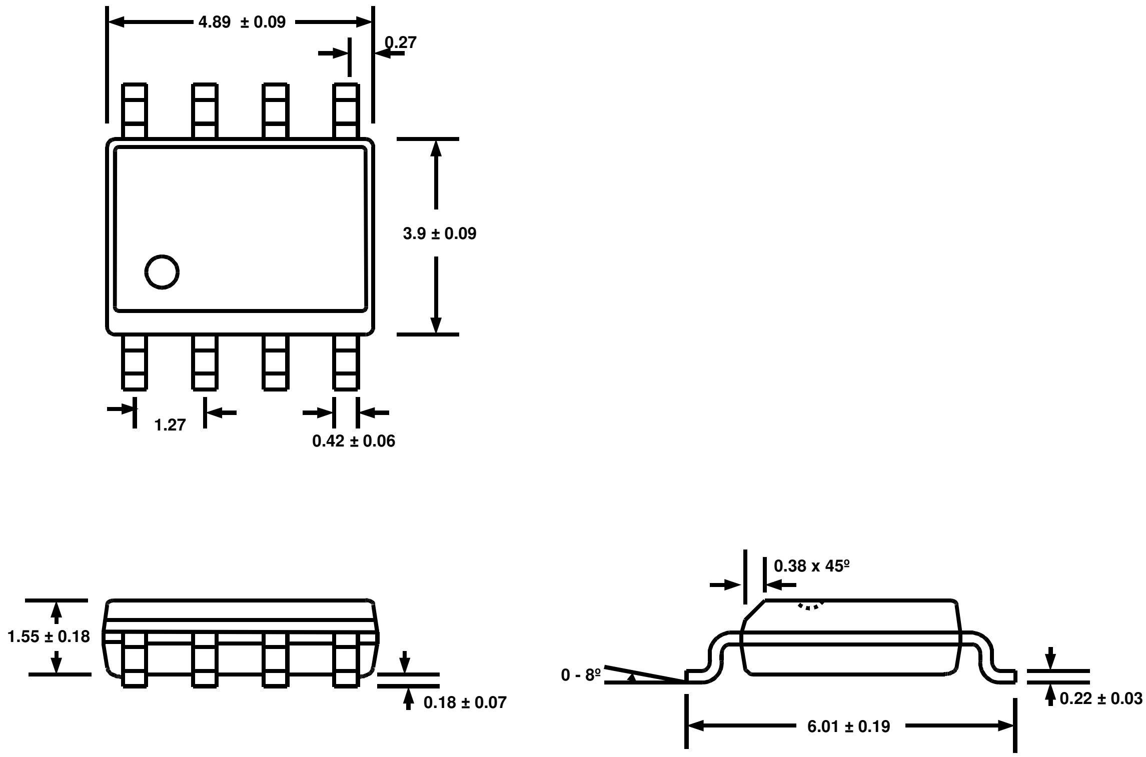
TX1, TX2 Pins

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On-state resistance	R_{TXON}	Pin current 10mA		1	2	Ω

PACKAGE INFORMATION

Package Dimensions

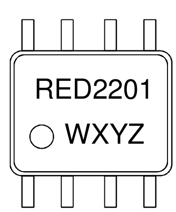
SO8 package dimensions are shown below. All units are in mm.



Available packages

Package type	Part number	Moisture Sensitivity Level (MSL)	Packaging
SO8	RED2201AD-TR13	3 (JEDEC J-STD-020)	Tape and reel 2500 / 13” reel

Package Marking



Part numbering for RED2201
RED2201:
RED = RediSem
2201= Part Number
WXYZ= Lot Code, e.g. AAAA, AAAB

The status of this Datasheet is shown in the footer.

Datasheet Status	Product Status	Definition
Preview	In development	The Datasheet contains target specifications relating to design and development of the described IC product.
Preliminary	In qualification	The Datasheet contains preliminary specifications relating to functionality and performance of the described IC product.
Production	In production	The Datasheet contains specifications relating to functionality and performance of the described IC product which are supported by testing during development and production.

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