RediSem CV PPFC LED Design Guide

Overview

RediSem's CSOC bipolar transistor technology enables high quality CV driver whilst keeping the cost low. RediSem's core technology is resonant power conversion, which means high efficiency and low EMI. This means that design times are short and it is easy to achieve a high-quality CV driver using either passive or active power factor correction.

RediSem's patented Passive Power Factor Control (PPFC) LED driver designs offer significant performance benefits over standard LED driver solutions. They use a unique single stage series-resonant converter with a charge-pump PFC circuit to give good power factor correction. These driver designs are naturally flicker free and are much lower cost than a 2-stage conventional design. RediSem's resonant converters designs use Bipolar transistors, which are highly efficient and resonant switching means low Electromagnetic Interference (EMI). The use of a high level of IC integration with controller IC's such as the RED2541 combined with low cost bipolar transistors offers a cost-competitive high-performance solution. RediSem solutions can also be used in conjunction with a 2-stage design incorporating Active PFC. In summary, the key features and benefits are:

- **RediSem Single Stage CV LED converter:**
  - Charge-pump PFC circuit
  - Low output voltage ripple
  - High efficiency
  - Low EMI
  - Constant Voltage Output
  - Bipolar transistor half-bridge

- **RediSem's CV LED Controller ICs:**
  - Over-Current Protection
  - Short-circuit protection
  - OTP (over-temperature) protection
  - Integrated bipolar transistor drive circuit
  - SO8 package

This design guide's aim is to explain the use of RediSem's controller ICs and CV LED driver application so that you can develop your own designs. It is recommended you always use one of RediSem's example designs as a starting point for new designs. Please check with us regularly for updates and additional information. As RediSem develops more CV LED driver example designs, this Design Guide will be updated from time to time.

Expected Performance

A typical 60W (24V 2.5A) LED CV driver achieves:

Efficiency (full load)	91%
Efficiency (10% load)	88%
No-load power	<250mW
Power Factor	0.98
Harmonic Distortion	<15% @ full load
Voltage Regulation	<1%
Current Limit	110%
Voltage Ripple	<1%

Passive Power Factor Correction (PPFC)

LED Drivers, especially those with input power >25W need a good Power Factor Correction and low THD to comply with limits for Power Factor and Harmonic Emissions. One common but expensive solution has been to use Active Power Factor Correction (APFC) which requires a separate switching Power Factor Correction block, with dedicated switching device and control circuit. The RediSem PPFC topology uses switching diodes to provide charge-pumping (boosting) to control Power Factor and Harmonic Emissions, without the need for another controller or any additional active switching devices.

Integrated CSOC and PPFC

Figure 1 shows the block diagram of RediSem's CV LED Driver which integrates RediSem's CSOC with the PPFC topology. The capacitive charge pumps form the PPFC stage, fitted in the return current path between the main transformer primary winding and the diode bridge block. The primary winding current drives the boosting and power factor correction. For a detailed explanation of RediSem's PPFC topology, please refer to AN2101.

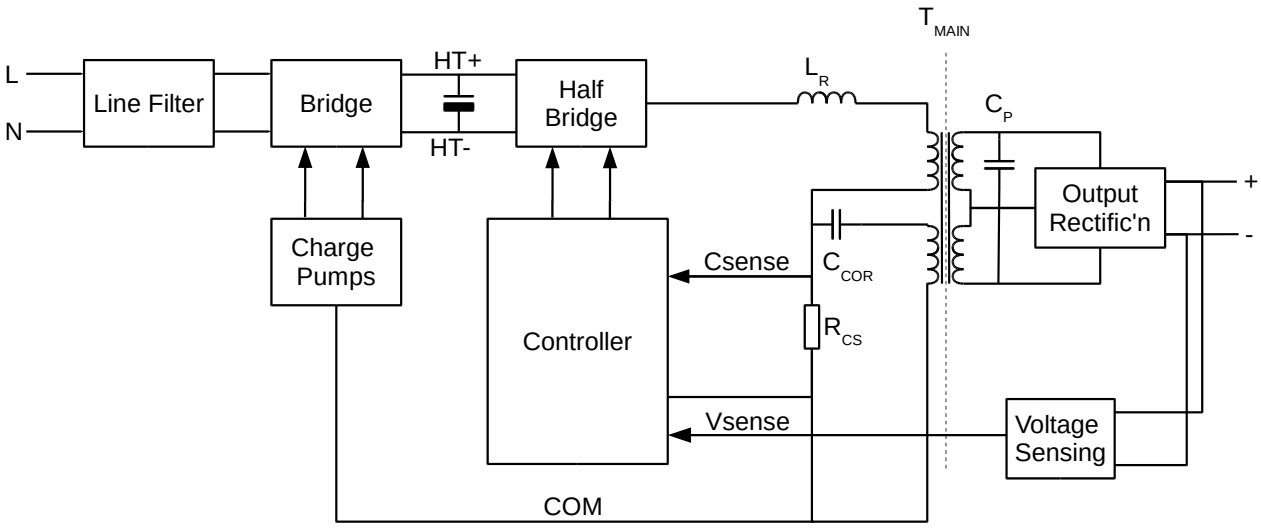

Figure 1: CSOC with PPFC

Using CSOC with Active Power Factor Correction (APFC)

For some applications, such as those with very wide input/output voltage requirements, it may be necessary to use APFC. RediSem's LED controller IC's may be easily combined with a third-party APFC pre-regulator design, as shown in Figure 2. Please consult the RediSem application note AN2111 for APFC design information.

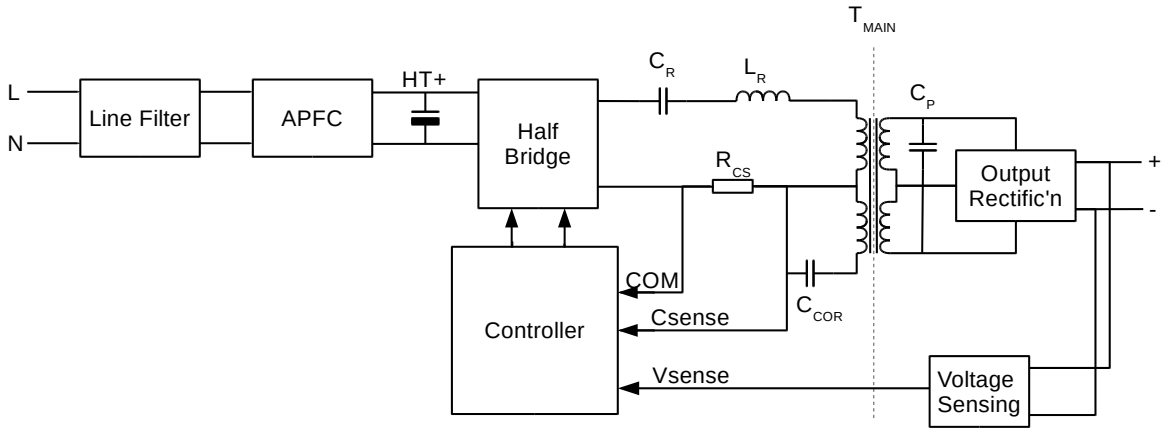

Figure 2: CSOC with APFC

The LCCC converter

Topology overview

The design described here combines a fully resonant LCCC half-bridge converter with integral PPFC to deliver a product which exceeds the performance of competing CV driver offerings, achieving full EMC compliance at a fraction of the cost. The RED2541 utilises an important feature of the topology, which is the ability of accurately sensing the output current from the primary side alone, which reduces costs and minimises losses.

Resonant LCCC Half-bridge

The resonant half-bridge LC topology can achieve high efficiency and excellent EMI at low cost. However, the LC topology is not well-suited for low-cost applications which require a wide load range. Alternatively, the LLC and LCC topologies can achieve a wider load range but are unsuitable for accurate primary-sensing of current. The LCCC topology described below (ref figure 1) can achieve high efficiency, excellent EMI and accurate primary-sensed current limiting.

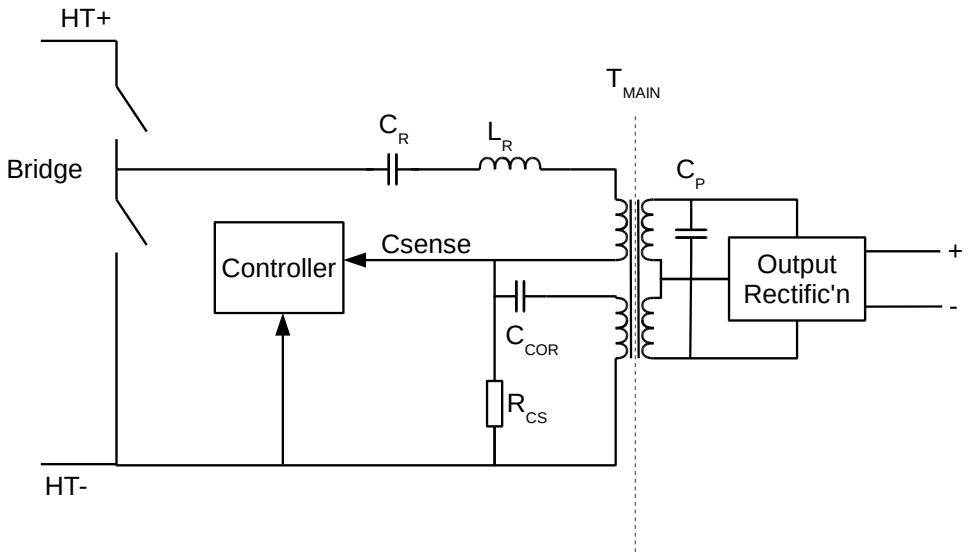

Figure 3: LCCC topology

The LCCC topology uses a LCC series/parallel resonant tank with capacitive current correction, totalling one inductance and three capacitors, hence the abbreviation LCCC. Components Cr, Lr provide the series resonance, while Lr and Cp provide the parallel resonance. By having multiple resonance points, the frequency range required for regulation is reduced, facilitating high efficiency across a wide load range. Capacitor Ccor provides correction to the current signal, cancelling out the transformed reactive current that flows through Cp, so that the current sense signal [CS] to the controller represents the pure load current.

Redisem Driver Controller ICs

RediSem's LED Driver Controller ICs are specifically designed for series-resonant topologies for LED Drivers. RediSem's controller ICs are unique in that they combine a self-oscillating bipolar converter (CSOC) topology with a simple half-bridge control scheme using bipolar switching devices, which are both lower cost and more robust than MOSFET alternatives. Furthermore, the self-oscillating design does not require dead-time controlto avoid hard switching, which can be a considerable problem for MOSFET-based solutions.

Differences from CC Driver Applications

No-load operation

The power output range for CV LED drivers is typically 0-100%, much wider than that for the CC LED drivers, which are generally require 50-100% output power range. Therefore, capacitor Cp is added across the secondary windings, to provide the additional reactive current to maintain oscillation at low loads.

The RED2541 controller is designed to switch into burst mode for loads below 5%, providing good low-load efficiency and low standby power. This burst level may be adjusted to any value within the range 0-10% as required. Note that burst mode is required for high efficiency at low loads, but if the level is set too high, bursting can clause audio noise.

Calculations of key CV components

The key component values of a CV driver application are easily scaled from one of RediSem's standard designs. The designer is recommended to use RediSem's Component Calculator spreadsheet – the design equations in the following sections are copied from this.

Additional components required for CV applications

There are some extra components required for CV applications:

- parallel resonance capacitor Cp (to handle the wider load range);
- correction capacitor Ccor (to cancel the reactive current created by Cp);
- secondary-side voltage sensing circuit and the optocoupler feedback (for accurate output voltage regulation);
- an auxiliary winding on main transformer to provide primary-sensed voltage feedback (as a backup in case the optocoupler fails).

Comparison of components which are common to both CC and CV Applications

Compared to the CC PPFC driver designs, there are several differences in the common components, as listed below:

- the Q factor of the resonant tank is slightly higher than the tank used in the CC drivers, so the inductance value is higher and the charge pump capacitor values are lower;
- the HT capacitor is slightly larger, to reduce the peak voltage stress;
- the output capacitor is larger, to achieve the required output voltage ripple;
- there are typically more charge pump blocks to achieve harmonics emissions compliance across the output load range (wider range in CV applications).

Detailed Design Notes RED2541

The following examples show how to scale this design to create a new application. Before starting a new design, check in the RediSem Apps library for the design which most closely meets your requirements. The schematic of a typical 60W CV LED Driver design is shown for reference in Figure *4*.

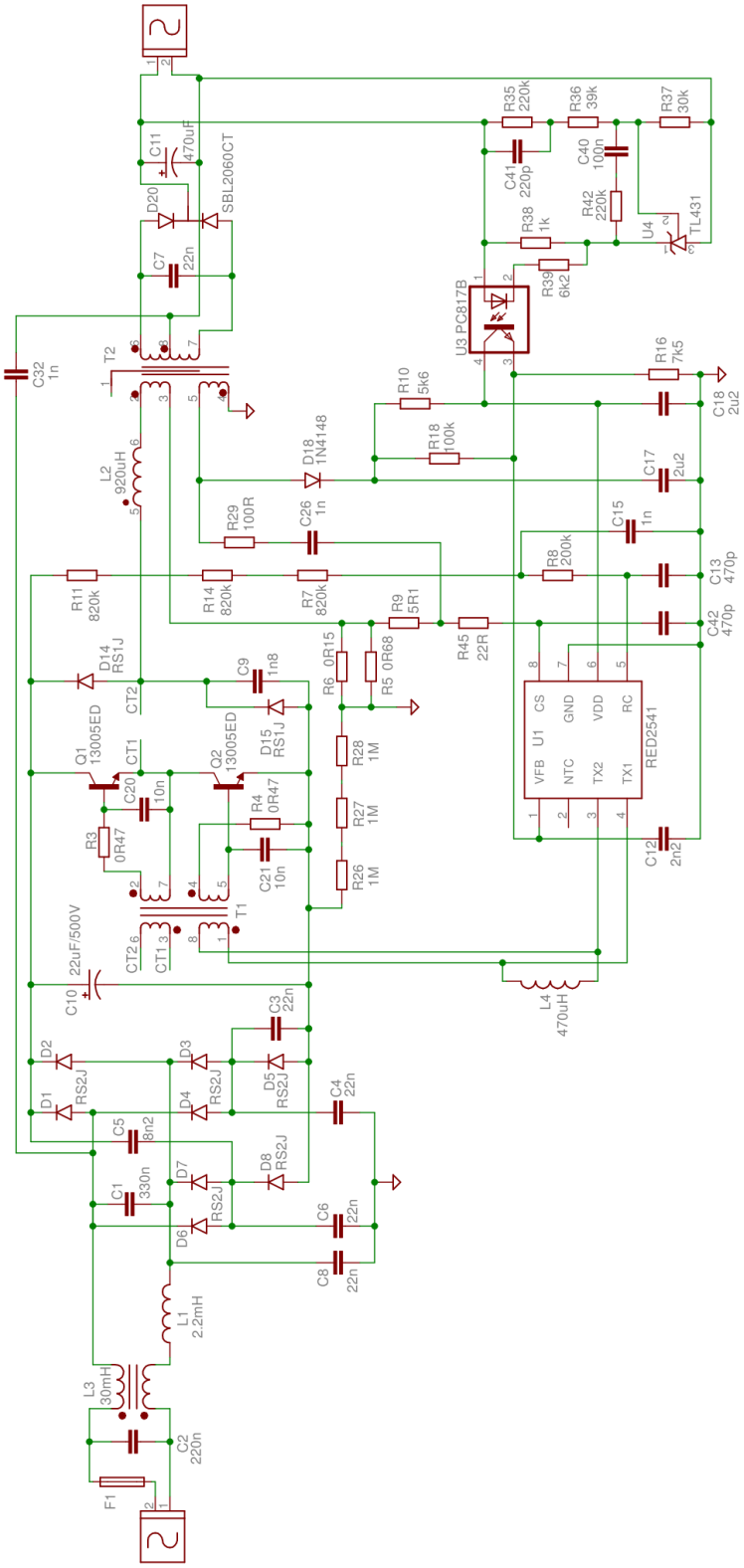

Figure 4: Schematic of 60W CV LED Driver with PPFC, using RED2541

Top Level Design Choices

Before starting detailed design work, define the top-level system requirements:

Parameters	Names	Typical Values
Minimum line input	$V_{IN(min)}$,	198Vac
Maximum line input	$V_{IN(max)}$	264Vac
Output regulation voltage	V_{OUT}	12V, 24V
Nominal power rating	P_{NOM}	20 - 100W
Minimum switching frequency	$F_{RES(target)}$	25 - 50kHz

Main Transformer

The desired transformer turns ratios are given by the following equations:

$$V_{PRIMAX} = \frac{V_{INMIN}}{2\sqrt{2}}$$

$$\frac{N_P}{N_S} < \frac{V_{PRIMAX}}{V_{OUT}}$$

$$\frac{N_A}{N_S} > \frac{V_{DDSTART(max)}}{VOUT} \times \frac{V_{REF}}{300mV}$$

Example

Application requirements:

V_{OUT} = 24V

V_{INMIN} = 198Vac

From IC datasheet:

$V_{DDSTART(max)}$ = 4.2V

V_{REF}=1.2V

Maximum primary winding voltage:

$$V_{PRIMAX} < \frac{198V}{2\sqrt{2}} = 72\ V$$

Primary/Secondary turns ratio:

$$\frac{N_P}{N_S} < \frac{72V}{24V} = 3$$

Aux/Secondary turns ratio:

$$\frac{N_A}{N_S} > \frac{4.2V}{24V} \times \frac{1.2V}{300mV} = 0.7$$

Transformer Construction

The recommended transformer design is shown in the figures below. Please note:

- if possible, the secondary windings should be wound together to minimise ringing
- the aux winding should be on top of the secondary windings, to optimise coupling to the secondary windings

More design advice is given in to AN2112: “LLC Transformer design for EMI”.

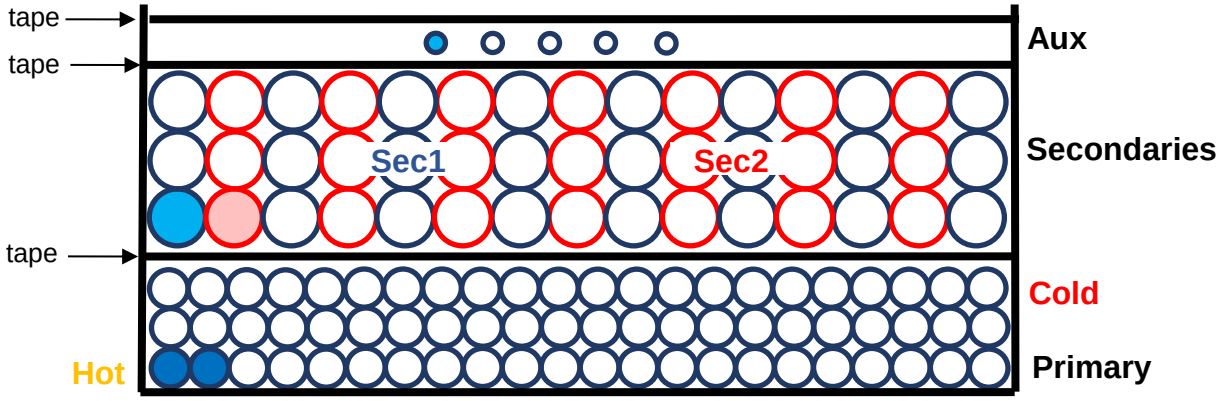

Figure 5: Typical Transformer Winding Arrangement

Resonant Components

If not already known, calculate the resonant frequency of the reference design, which is also the minimum operating frequency:

$$F_{RES(ref)} = \frac{1}{2\pi\sqrt{L_{2(ref)}\left(C_{4(ref)} + C_{6(ref)} + C_{8(ref)}\right)}}$$

Then calculate the primary and secondary capacitor scaling factors, Kcp and Kcs:

$$K_{CP} = \frac{P_{NOM(target)}}{P_{NOM(ref)}} \times \frac{F_{RES(ref)}}{F_{RES(target)}} \times \left(\frac{V_{INMIN(ref)}}{V_{INMIN(target)}}\right)^2$$

$$K_{CS} = \frac{P_{NOM(target)}}{P_{NOM(ref)}} \times \frac{F_{RES(ref)}}{F_{RES(target)}} \times \left(\frac{V_{OUT(ref)}}{V_{OUT(target)}}\right)^2$$

Now calculate the target value for each resonant capacitor, using Kcs for the secondary resonant capacitor and Kcp for the others. For example, if $C_{3(ref)}$ is the value of C_3 in the reference design, choose the nearest available value for C_3 for the new design from the following equation:

$$C_3 = C_{3(ref)} \times K_{CP}$$

The resonant inductor value L_2 should be chosen using the following equation:

$$L_2 = L_{2(ref)} \times \frac{P_{NOM(ref)}}{P_{NOM}} \times \frac{F_{RES(ref)}}{F_{RES(target)}} \times \left(\frac{V_{INMIN}}{V_{INMIN(ref)}}\right)^2$$

Now, calculate the actual resonant frequency:

$$F_{RES} = \frac{1}{2\pi\sqrt{L_2(C_4+C_6+C_8)}}$$

Example

Application requirements:

$P_{NOM(target)}$ = 50 W
$F_{RES(target)}$ = 25 kHz
V_{INMIN} = 198Vac
V_{OUT} = 12Vdc

Calculate resonant frequency of reference design:

$$F_{RES(ref)} = \frac{1}{2\pi\sqrt{920uH(22n+22n+22n)}} = 20.4 \text{ kHz}$$

Calculate capacitor scaling factors:

$$K_{CP} = \frac{50W}{60W} \times \frac{20.4k}{30k} \times [\frac{198V}{198V}]^2 = 0.681$$
$$K_{CS} = \frac{50W}{60W} \times \frac{20.4k}{30k} \times [\frac{24V}{12V}]^2 = 2.72$$

Calculate target primary capacitor values:

$C_3 = 22 \times 0.708 = 15.6 \approx 15\text{nF}$
$C_4 = 22 \times 0.708 = 15.6 \approx 15\text{nF}$
$C_5 = 8.2 \times 0.708 = 5.8 \approx 5.6\text{nF}$
$C_6 = 22 \times 0.708 = 15.6 \approx 15\text{nF}$
$C_8 = 22 \times 0.708 = 15.6 \approx 15\text{nF}$

Calculate target secondary capacitor values:

$C_7 = 22 \times 2.72 = 60 \approx 56\text{nF}$

Calculate resonant inductor value:

$$L_2 = 920uH \times \frac{60W}{50W} \times \frac{20.4k}{25k} \times [\frac{198V}{198V}]^2 = 902uH$$

Estimate actual resonant frequency:

$$F_{RES} = \frac{1}{2\pi\sqrt{902u(15n+15n+15n)}} = 25.0 \text{ kHz}$$

Controller IC

Supply Rails

The control IC's incorporate a low power shunt regulator, which normally maintains the V_{DD} supply rail at voltage V_{DDREG} and requires supply current I_{DDRUN}. The controller IC will shut down if the VDD supply drops below $V_{UVD.}$ The value of R_{10} is chosen to maximise the holdup time of the VDD rail, and is determined by the equations below:

$$V_{AUX} = \frac{N_A}{N_S}.V_{OUT} - V_{DIODE}$$

$$R_{10} = \frac{V_{AUX} - V_{DDREG(max)}}{2.72 \times I_{DDRUN(max)}} \Omega$$

Example
Application parameters:

$V_{OUT} = 12$ V
$V_{DIODE} = 0.6$ V
$V_{DDREG(min)} = 3.3$ V (from datasheet)
$V_{DDREG(max)} = 3.6$ V (from datasheet)
$I_{DDRUN(max)} = 800$ uA (from datasheet)

Auxiliary rail voltage:
$V_{AUX} = 0.7 \times 12V - 0.6V = 16.2$V

R_{10} value:
$R_{10} = \frac{16.2V - 3.6V}{2.72 \times 800uA} \approx 5.6k\Omega$

The value of C_{18} is sized to hold up the VDD supply rail during start up, and is typically 2.2uF.

The value of C_{17} determines the minimum burst frequency at no loads. A lower frequency helps to minimise standby power, but increases the startup time. Typically choose $F_{BURST} \approx 200$Hz.

$$C_{17} \approx \frac{1}{R_{10} \times F_{BURST} \times \ln\left(\frac{V_{AUX}}{V_{DDSA(max)} + R_{10} \times I_{DDRUN(max)}}\right)}$$

Example
Application requirements:

$F_{BURST} = 200Hz$
$R_{10} = 5.6k\Omega$
$V_{AUX} = 16.3V$

From RED2541 datasheet:

$V_{DDSA(max)} = 3.07$V
$I_{DDRUN(max)} = 800$uA

$$C_{17} \approx \frac{1}{5.6kx200Hz \times \ln\left(\frac{16.3V}{3.07V + 5.6k \times 800uA}\right)} \approx 1uF$$

Startup Resistors

At startup, the VDD rail is charged up by resistor chains [R_7, R_{11}, R_{14}, R_8] and [R_{26}, R_{27}, R_{28}]. The value of R_8 is preferred to be 200kΩ.The values of the others depend primarily upon the combined capacitance connected to the VDD and AUX supply rails and the required startup time, $t_{STARTUP}$:

$$R_7 + R_8 + R_{11} + R_{18} + R_{26} + R_{27} + R_{28} = R_{BOOTTOTAL} < \frac{t_{STARTUP} * V_{INMIN}}{(C_{17} + C_{18}) * V_{DDSTART}}$$

Example
Application requirements:

$t_{STARTUP} = 450ms$ (max)
$V_{INMIN} = 198Vac$
$C_{17} = 1uF$
$C_{18} = 2.2uF$

From RED2541 datasheet

$V_{DDSTART} = 4.2V$(max)

$R_{BOOTTOTAL} < \frac{450m*198V}{(2.2u+1u)*4.2V} = 6.02\text{M}\Omega$

Hence choose resistor values:

$R_{26} = R_{27} = R_{28} = 1\ \text{M}\Omega$
$R_7 = R_{11} = R_{14} = 820k\Omega$

Timing Components

The minimum oscillator frequency is determined by C_{13} and [R_7+R_8+R_{11}+R_{14}]. The optimum value for C_{13} is given by the equation below:

$$C_{13} = \frac{1}{R_7 + R_8 + R_{11} + R_{14}} \times \frac{V_{AC(min)}}{\sqrt{2} \times 2.35V} \times \left(\frac{1}{2 \times F_{RES}} - t_{RCRST}\right)$$

Example
Application requirements:

$F_{RES} = 25kHz$

From above:

$R_8 = 200k\Omega$
$R_7 = R_{11} = R_{14} = 820k\Omega$

From datasheet:

$V_{RCMAX} = 2.35V$

$$C_{13} = \frac{1}{820k + 200k + 820k + 820k} \times \frac{198\text{V}}{\sqrt{2} \times V_{RCMAX}} \times \left(\frac{1}{2 \times 25k} - 0.7u\right) \approx 470pF$$

Booting Up

R_{19} prevents the controller from trying to start up when the line voltage is too low. The optimum value for R_{19} is given by:

$$R_{19} > \frac{V_{DDSTART}}{\left(\frac{V_{ACBOOT}}{R_{BOOTTOTAL}} - I_{DDSLEEP}\right)}$$

Example
Application requirements:

$V_{DDSTART(max)} = 4.2V$
$C_{13} = 470pF$
$V_{ACBOOT(min)} = 180Vac$

RED2541 datasheet:

$I_{DDSLEEP(max)} = 12uA$
$V_{DDSTART(max)} = 4.2V$

$$R_{19} > \frac{4.2V}{\left(\frac{\sqrt{2}\times 180V}{200k+820k+820k+820k+1M+1M+1M} - 12uA\right)} \approx 220k\Omega$$

Current Sensing Resistor

Typically, the overcurrent protection threshold is chosen to be about 15% bigger than the maximum load current. Therefore, the theoretical value of the current sense resistor R_6 is given by the equation below:

$$R_5 = 0.85\times\frac{N_P}{N_S}\times\frac{V_{OUT}}{P_{NOM}}\times V_{CSREG}$$

Example
Application parameters:

$N_P = 41$ turns
$N_S = 7$ turns
$Pnom = 50W$
$Vout = 12V$

RED2541 datasheet parameters:

$V_{CSREG} = 100mV$

$$R_5 = 0.85\times\frac{N_P}{N_S}\times\frac{12V}{50W}\times 100mV = 0.12\Omega$$

Load Pull-up

The CS pin is connected to the current sensing resistor R_5 via padding resistor R_{45} (typically 22Ω). R_{45} is used to increase the output current limit I_{OUTPK} during startup, to help pull up difficult loads. The value of R_{45} is chosen according to the following equation:

$$R_{45} = R_{CSPD}\times\left(\frac{I_{OUTPK}\times R_5}{V_{CSREG2}}\times\frac{N_S}{N_P} - 1\right)$$

Example
Application parameters:

$I_{OUTPK} = 6.4A$
$R_{CS} = 0.12\Omega$
$N_P = 41$ turns
$N_S = 7$ turns

From RED2541 datasheet:

$R_{CSPD2} = 200\mathrm{R}$
$V_{CSREG2} = 118mV$

$$R_{45} = 200R\times\left(\frac{6.4A\times 0.12R}{118mV}\times\frac{9}{41} - 1\right) \approx 22\Omega$$

Current Correction Network

Components C_{26} and R_9 correct the CS signal by removing the reactive current which is induced by the parallel resonance capacitor C_P. The capacitor C_{26} is normally chosen to be 1nF (5% COG/NPO). R_{29} provides damping to suppress ringing in the CS waveform, value usually 100R. The value of R_9 is given by the equation below:

$$R_9 = R_5 * \left[\frac{C_7}{C_{26}} * \frac{4*N_S^2}{N_A*N_P} - 1\right]$$

Example
Application parameters:

$C_7 = 15n$
$C_{26} = 1n$
$R_5 = 0.12\Omega$
$N_P = 41$ turns
$N_S = 7$ turns
$N_A = 9$ turns

$$R_9 = 0.12R \times \left(\frac{15n}{1n} \times \frac{4\times7^2}{41\times9} - 1\right) \approx 3.3\Omega$$

Voltage Control Loop

In normal operation, accurate voltage regulation is provided by a voltage reference IC (e.g. TL431) located on the secondary side. For protection against optocoupler faults, primary voltage sensing is also provided as a backup measure, by sensing the auxiliary supply rail.

Primary voltage sensing

R_{18} and R_{16} provide simple voltage feedback from the Aux supply rail to the VFB pin, limiting the output voltage in case the optocoupler fails. A small margin is applied to ensure that the primary voltage sensing does not interfere with the secondary voltage regulation during normal operation.
R_{16} is typically chosen to be 7.5kΩ. The optimum value for R_{18} is given by the equation below:

$$R_{18} = R_{16} * \left[\frac{V_{OUT} * N_A/N_S}{V_{REF}} - 1\right] * 1.15$$

Example
Application parameters:

$R_{16} = 7.5\text{k}$
$V_{OUT} = 12\text{V}$
$V_{REF} = 1.2\text{V}$
$N_P = 41$ turns
$N_S = 7$ turns
$N_A = 9$ turns

$$R_{18} = 7.5k * \left(\frac{12V*9/7}{1.2V} - 1\right) * 1.15 \approx 100\text{k}\Omega$$

For suppression of noise, it is usually necessary to include a simple low-pass filter, provided by R_{41} and C_{12}. Recommended values are R_{41}=10k and C_{12}=2.2nF. If other values are chosen, ensure that the secondary voltage sensing circuit has correct compensation to maintain stability.

Optocoupler

U_3 transfers the analogue feedback signal from the secondary sensing circuit to the control IC on the primary side. Any low-cost analogue optocoupler can be used, provided that the current transfer ratio (CTR) is defined.

Secondary voltage sensing

The output voltage is sensed by a voltage regulator IC (e.g. TL431 or similar) located on the secondary side, which drives the optocoupler.

There are many ways in which the compensator can be configured, depending on the required performance. Two configurations are presented here:

1) Normal loop for low ripple;
2) Slow loop for PWM-switched LED loads, to minimise audio noise.

Normal loop configuration – for low ripple

The voltage regulation circuit around the TL431 is a proportional-integral-derivative (PID) configuration, as shown in Figure 6.

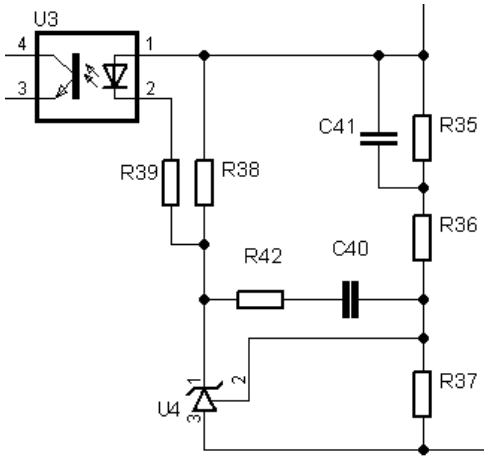

Figure 6: Secondary voltage sensing - normal loop configuration

The loop compensation depends on the value of the output capacitor, C_{11}. The recommended value for C11 is given by:

$$C_{11} = 3000u \times \frac{P_{NOM}}{V_{OUT}^2}$$

Then, the optimum loop compensation values are given by the following equations.

$$R_{37} = 30k$$

$$R_{35} = R_{37}.\left(\frac{V_{OUT}}{V_{REF}} - 1\right).\frac{5}{6}$$

$$R_{36} = R_{37}.\left(\frac{V_{OUT}}{V_{REF}} - 1\right) - R_{35}$$

$$R_{38} = \frac{1}{50}.\frac{V_{OUT}}{C_{11}}$$

$$R_{39} = \frac{1}{40}.\frac{P_{NOM}}{C_{11}}.CTR_{MAX}$$

$$R_{42} = 45M.\frac{C_{11}.V_{OUT}^2}{P_{NOM}}$$

$$C_{40} = 450p.\left(\frac{P_{NOM}}{C_{11}.V_{OUT}^2}\right)$$

$$C_{41} = \frac{30u + C_{12}.(R_{16} + R_{41})}{R_{35}}$$

Example

Application parameters:

$V_{OUT} = 12V$
$V_{REF} = 2.5V$
$P_{NOM} = 50W$
$CTR_{MAX} = 260\%$

$$C_{11} = 3000u \times \frac{50W}{12V^2} \approx 1000uF$$

$$R_{37} = 30k$$

$$R_{35} = 30k.\left(\frac{12V}{2.5V} - 1\right).\frac{5}{6} \approx 91k$$

$$R_{36} = 30k.\left(\frac{12V}{2.5V} - 1\right) - 91k \approx 22k$$

$$R_{38} = \frac{1}{50}.\frac{12V}{1000u} \approx 240\Omega$$

$$R_{39} = \frac{1}{40}.\frac{50W}{1000u}.260\% \approx 3.3k$$

$$R_{42} = 45M.\frac{1000u.12V^2}{50W} \approx 130k$$

$$C_{40} = 450p.\left(\frac{50W}{1000u.12V^2}\right) \approx 150n$$

$$C_{41} = \frac{30u + 2n2.(10k + 7k5)}{91k} \approx 680p$$

Slow loop configuration – for PWM-switched LED loads

LED dimming methods which use load chopping are likely to generate audible noise at the chopping frequency (typically ~1kHz). The noise level emanates from the resonant components, specifically L_2, C_2, C_4, C_5, C_6, C_7, C_8 and is very dependent on the depth of current modulation. Using a slower control loop reduces the current modulation depth, suppressing the noise.

The voltage regulation circuit around the TL431 is a modified proportional-integral-derivative (PID) configuration, as shown in Figure 7.

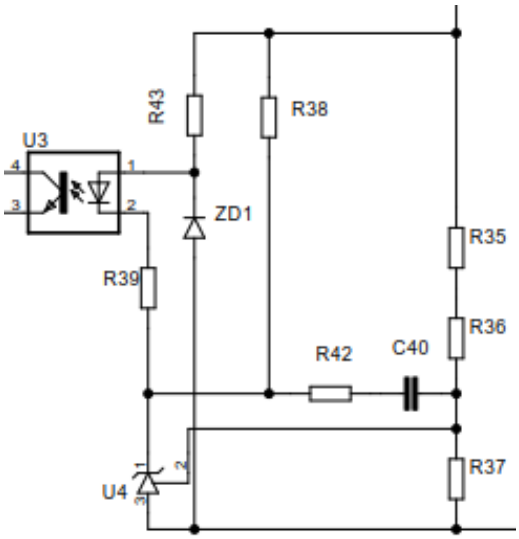

Figure 7: Secondary voltage sensing - slow loop configuration

The loop compensation depends on the value of the output capacitor, C_{11}. The recommended value for C11 is given by:

$$C_{11} = 3000u \times \frac{P_{NOM}}{V_{OUT}^2}$$

Then, the optimum loop compensation values are given by the following equations.

$$ZD_1 = \frac{3}{4} \times V_{OUT}$$

$$R_{37} = 30k$$

$$R_{35} = R_{37}.\left(\frac{V_{OUT}}{V_{REF}} - 1\right).\frac{5}{6}$$

$$R_{36} = R_{37}.\left(\frac{V_{OUT}}{V_{REF}} - 1\right) - R_{35}$$

$$R_{38} = \frac{1}{50}.\frac{V_{OUT}}{C_{11}}$$

$$R_{39} = \frac{1}{40}.\frac{P_{NOM}}{C_{11}}.CTR_{MAX}$$

$$R_{42} = 1M.\frac{C_{11}.V_{OUT}^2}{P_{NOM}}$$

$$R_{43} = \frac{V_{OUT} - ZD_1}{1m}$$

$$C_{40} = 450p.\left(\frac{P_{NOM}}{C_{11}.V_{OUT}^2}\right)$$

$$C_{41} = \frac{30u + C_{12}.(R_{16} + R_{41})}{R_{35}}$$

Example

Application parameters:

$V_{OUT} = 12V$
$V_{REF} = 2.5V$
$P_{NOM} = 50W$
$CTR_{MAX} = 260\%$

$$C_{11} = 3000u \times \frac{50W}{12V^2} \approx 1000uF$$

$$ZD_1 = \frac{3}{4}.12V \approx 8.2V$$

$$R_{37} = 30k$$

$$R_{35} = 30k.\left(\frac{12V}{2.5V} - 1\right).\frac{5}{6} \approx 91k$$

$$R_{36} = 30k.\left(\frac{12V}{2.5V} - 1\right) - 91k \approx 22k$$

$$R_{38} = \frac{1}{50}.\frac{12V}{1000u} \approx 240\Omega$$

$$R_{39} = \frac{1}{40}.\frac{50W}{1000u}.260\% \approx 3.3k$$

$$R_{42} = 1M.\frac{1000u.12V^2}{50W} \approx 3k$$

$$R_{43} = \frac{12V - 8.2V}{1m} \approx 3.9k$$

$$C_{40} = 450p.\left(\frac{50W}{1000u.12V^2}\right) \approx 150n$$

$$C_{41} = \frac{30u + 2n2.(10k + 7k5)}{91k} \approx 680p$$

Protection Features

Capacitive Mode Protection

CSOC converters are not able to operate in capacitive mode. The base drive transformer (in conjunction with the IC) will prevent the converter operating in capacitive mode. Good designs will ensure that the converter does not enter capacitive mode in normal operation. If the base drive inductance is not enough, the transistors can turn off prematurely. If this occurs, the capacitive mode protection feature in the IC will become active and the base drive transformer will effectively set the converter operating frequency.

Short circuit protection (SCP)

When output terminals are short circuited, the VDD supply rail collapses and the IC restarts, initially at 50% current limit, to prevent excessive boosting of the HT capacitor voltage.

Over Current Protection (OCP)

If the output current continuously exceeds the OCP threshold, the IC latches a fault and shuts down and performs 7 dummy reboot cycles and attempts to reboot on the 8th cycle.

Over Temperature Protection (OTP)

IC has an internal over temperature shutdown level (see datasheet for details of OTP trip point). The IC shuts down and performs 7 dummy reboot cycles and attempts to reboot on the 8th cycle.

Remote Over-Temperature Protection
The IC can be shut down by connecting a negative temperature coefficient thermistor (NTC) or other external circuit to pin 2. If the voltage at pin 2 is less than 700mV, the IC shuts down, registering a fault. An internal current source on pin 2 is provided to sense the resistance of an NTC connected between pin 2 and GND. Internal hysteresis ensures that the NTC must cool down before the IC attempts to restart. Internal blanking allows a small capacitor to be fitted in parallel with the NTC, to suppress noise.

Half-Bridge Block

For detailed information on RediSem's CSOC and transistor drive technology, please consult AN2113. This document explains the circuit operation and component requirements for RediSem's patented half-bridge arrangement.

Base drive Transformer (T_1)

RediSem's designs are based on CSOC (Controlled Self-Oscillating Converter) technology. This means that it is like a self-oscillating design where the IC is in control of the frequency which regulates the output. Very importantly, the base drive transformer does not control the frequency of the converter, the IC does. The base drive transformer is only necessary to provide power to the transistors. Changing the number of turns or core material will not affect driver's operating power, but it will affect transistor temperature and operating performance at extreme temperatures and line/load combinations. Please be cautious when changing anything relating to the base drive transformer. Base drive transformer may be procured fully assembled and tested from Acme Electronics (越丰电子（广州）有限公司). For further details, please see AN2113.

Transistor choice (Q1, Q2)

Transistor choice is important in RediSem's LED driver solutions. Please begin by using transistors that RediSem recommends. When selecting other transistors, choose transistors with low fall time (t_f) and low storage times (t_s). Also, do not use transistors that are too big as larger transistors typically have higher switching losses. RediSem typically chooses transistors with a continuous collector current rating that is 2-3 times higher than the peak current the transistor sees in normal operation.

Base Resistors

The base resistor values affect the transistor storage and fall times. Choose large base resistor values to achieve fast turn-off times. However, make sure that the reflected drive voltage appearing on the Tx pins of the controller IC does not exceed the datasheet limits (4V).
As a starting point, choose the value for the base resistors from the following equation:

$$R_3 = R_4 = \frac{40W}{P_{OUT}} \times \frac{V_{IN}}{230V}\ \Omega$$

Flywheel Diodes

D_{14} and D_{15} provide a route for the primary magnetizing current to return to the HT+ and HT- supply rails. The types chosen should be fast turn on and fast recovery to ensure snap-free commutation. (Note that most datasheets do not specify turn-on time). If these diodes have too slow turn-on, it can cause switching transistors Q1, Q2 to run hot, due to shoot-through current spikes. Good diode types are HS1J available from Taiwan Semi (台湾半导体有限公司).

Mid-point capacitor (C_9)

There is a mid-point capacitor on the half-bridge output which helps to reduce switching losses in the transistors and suppress RF emissions. The capacitor must be NPO or COG. It should be rated for 4x nominal line voltage. As a starting point, use the following equation:

$$C_9 = 1n \times \frac{60W}{P_{OUT}} \times \frac{V_{IN}}{230V}\ \text{F}$$

Bulk Capacitor (C_{10})

For PPFC applications, the peak voltage appearing on the bulk capacitor C_{25} can reach as much as 150% of peak line voltage under worst case conditions (high line, low load). As starting point, choose a 500V rated capacitor according to the following equation:

$$C_{10} = 15u \times \frac{60W}{P_{OUT}} \times \frac{V_{IN}}{230V} \text{ F}$$

If space permits, it may be better to use to use two identical capacitors in series to achieve the necessary voltage rating at low cost.

Line Input Protection

For overcurrent protection, a conventional fuse is recommended, with adequate current rating and slow rupture characteristics to withstand High Energy Surge tests. Alternatively, a 2R2 fuse resistor may be used, but this will reduce the overall efficiency and increase the internal case temperature.

Additional protection against line Over-Voltage conditions, such as High Energy Surges, is normally not required, as the design already has line filtering directly on the line input. Additionally, the half-bridge topology used here has plenty of voltage headroom on the switching devices (unlike typical flyback designs).

Inrush current limiting is provided by the inherent resistance of the line filter block, in particularly the common-mode choke.

Surge components

RediSem solutions use a half-bridge configuration with 700V transistors (V_{CES}). This means that the transistors can survive with an HT bus voltage of up to 700V. Passing a 500V or 1kV differential surge requirement therefore means keeping the HT bus below 700V during a surge, or below 650V to have some margin. The HT capacitor combined with the input impedance (resistance of the fuse-resistor as well as CM and DM chokes) is usually enough to resist the surge, but an MOV can also be added if the input impedance is small.

Be very careful during surge testing and use proper safety precautions.

EMI Measures

Line Filtering

Conducted RF Emissions are suppressed by a differential-mode choke, a common-mode choke and two class-X capacitors. Note that if the class-X capacitors are made too large, the Power Factor will be reduced.

Snubber

A secondary snubber can improve RF emissions in the range 5-15MHz.

Y-Capacitor

It should not be necessary to use a class “Y” capacitor across the isolation barrier if care is taken when designing the transformer. Ensure that the secondary windings are adequately screened from the primary circuit.

PCB Layout

Ground Star Point

The CS pin is sensitive to noise injected from surrounding components and tracks. Treat the COM end of the current-sense resistor (R_5) as the COM star point between the controller block and the power circuit, to

avoid noise induced by switching current loops (see Figure 8). Keep the track length to the CS pin as short as possible. Do not pass the main load current underneath the IC.

Keep the Aux power loop small. The loop from the Aux winding, passing through D_{18}, C_{17} and returning to the transformer winding should be short. The GND return from C_{17} does not have to be connected back to the star point.

High voltage nodes

Be careful to minimise track lengths of high voltage nodes and keep these well away from the control IC. If using a drum core for the resonant inductor (L_2), note that the hot end (i.e. the end connected to Q_1, Q_2) can couple noise into the control IC. Also keep the drum core apart from any magnetic EMI components to avoid EMI problems due to unwanted magnetic coupling.

Sensitive Nodes

Tracking of sensitive circuit nodes, particularly pins 1, 5 and 8 (VFB, RC and CS inputs) of the controller IC should be protected by a ground plane and distanced well away from hot nodes, such as the switching BJTs and the resonant inductor. These tracks should be kept short, as noted in the example schematic in Figure 8

Keep R_8 and C_{13} close to the IC, minimising the length and area of the RC pin tracking.

V_{DD} decoupling capacitor

Keep the power tracks to the decoupling capacitor C_{18} very short.

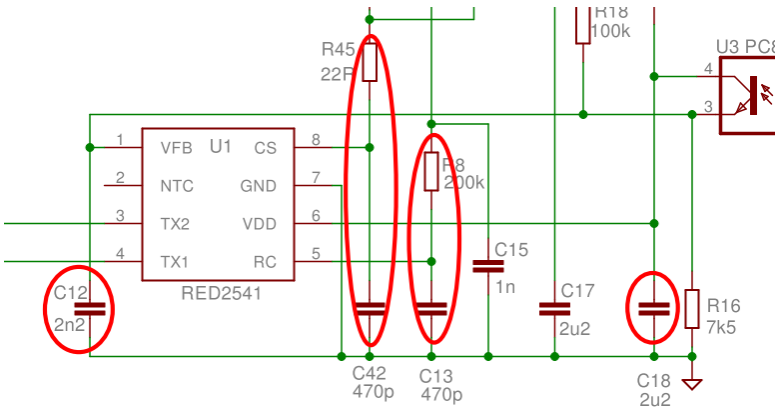

Figure 8: Keep tracks to these components short

About RediSem

RediSem designs and supplies semiconductor ICs for energy efficient power management applications. RediSem uniquely combines extensive experience in power electronics with in-depth knowledge of IC design and manufacturing and works with the world's top suppliers and customers. RediSem's unique patented IC and converter technologies deliver maximum efficiency and performance, while reducing overall bill of materials cost through the use of bipolar transistors.

RediSem's range of LED control ICs can be used with RediSem's patented single stage LED control solution to provide very high efficiencies with low EMI – all with a single IC. When combined, these features deliver a low cost, high performance LED driver solution.

RediSem's fluorescent driver controller ICs achieve the advanced performance of MOSFET drivers by using bipolar transistors at a fraction of the BOM cost. RediSem's range of SMPS (Switched Mode Power Supply) control ICs enables low-cost LLC converters with bipolar transistors that deliver very high efficiencies already meeting DoE Level VI regulations, have low standby power and have much lower EMI compared to flyback converters.

All RediSem ICs are supported by comprehensive turn-key application designs enabling rapid time to market. For further information please use our contact details below

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