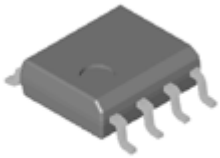
RED1401

PSR Controller for LLC converters

Features

- Advanced Controller IC for low-cost LLC converters with bipolar transistors
- PSR - Primary Side Regulation of output voltage and current without an opto-coupler
- 50% duty cycle, variable frequency control of resonant half-bridge
- Automatic dead-time control and capacitive mode protection
- Adjustable cable compensation
- Triple-mode over-current protection:
  - Programmable CC mode,
  - Cycle-by-cycle over-current protection
  - Hiccup overload protection
- Control Loop Fault protection
- Over-temperature protection
- Small SO8 IC package



SO8

Applications

- High Efficiency Adapters 5-30W
- Low-cost embedded Power Supplies 5-30W

Order code

Part Number	Package	Packaging
RED1401AD-TR13	SO8	Tape and reel

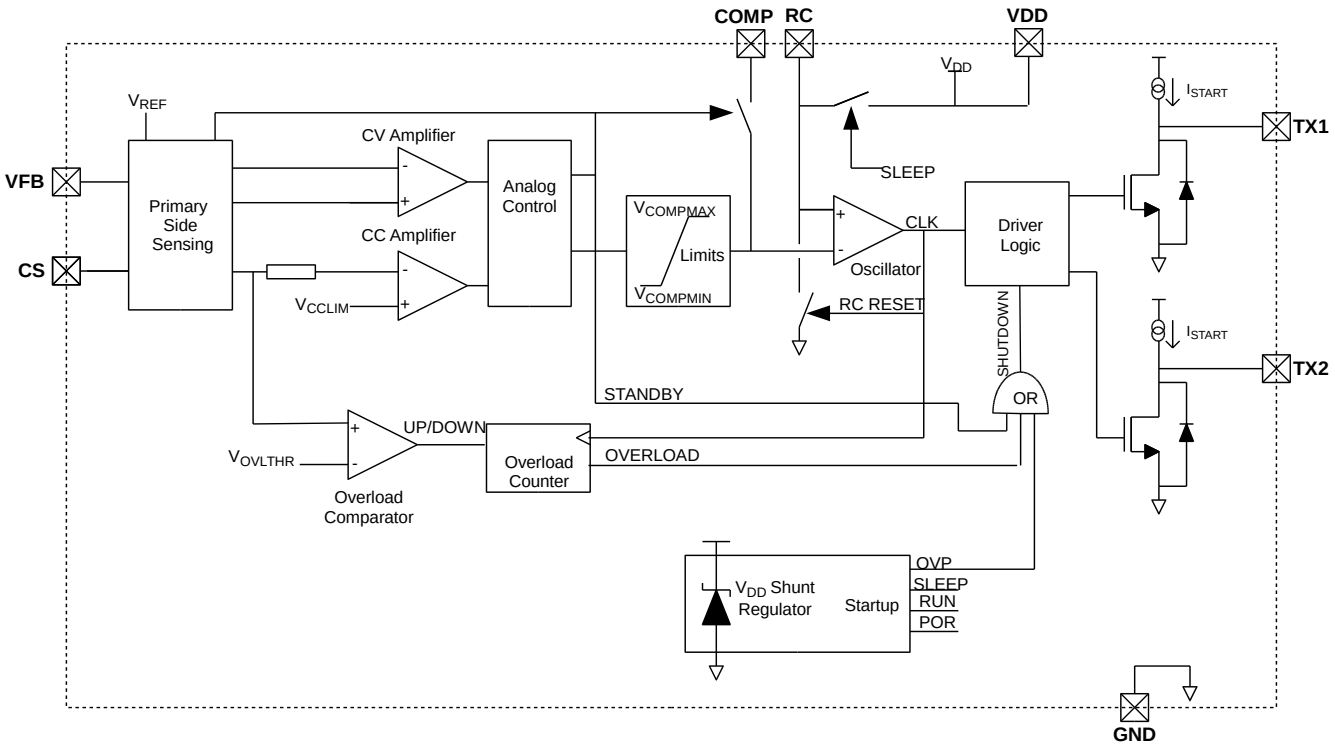


Figure 1: Block diagram

Device Pins

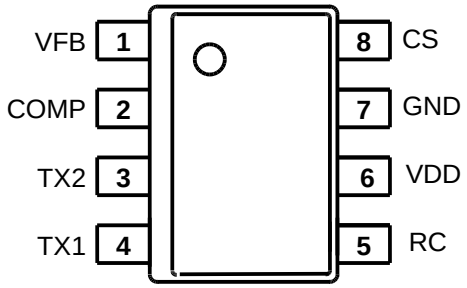


Figure 2: SO8 pin connections (top view)

Pin Functions

Pin #	Name	Function
1	VFB	PSR Feedback input for output voltage regulation. Connect to primary sense winding.
2	COMP	Buffered output of the control amplifiers. A loop compensation network connected between this pin and the VFB input defines CV mode loop response.
3	TX2	Output to control transformer.
4	TX1	Output to control transformer.
5	RC	External RC network sets the minimum [full power] switching frequency.
6	VDD	IC Power Supply pin – nominally 3.45V
7	GND	Chip ground.
8	CS	PSR Current Sense input provides output current limiting, cycle-by-cycle over-current protection and delayed overload protection. The CS pin is connected to the half-bridge current sense resistor

Typical Application

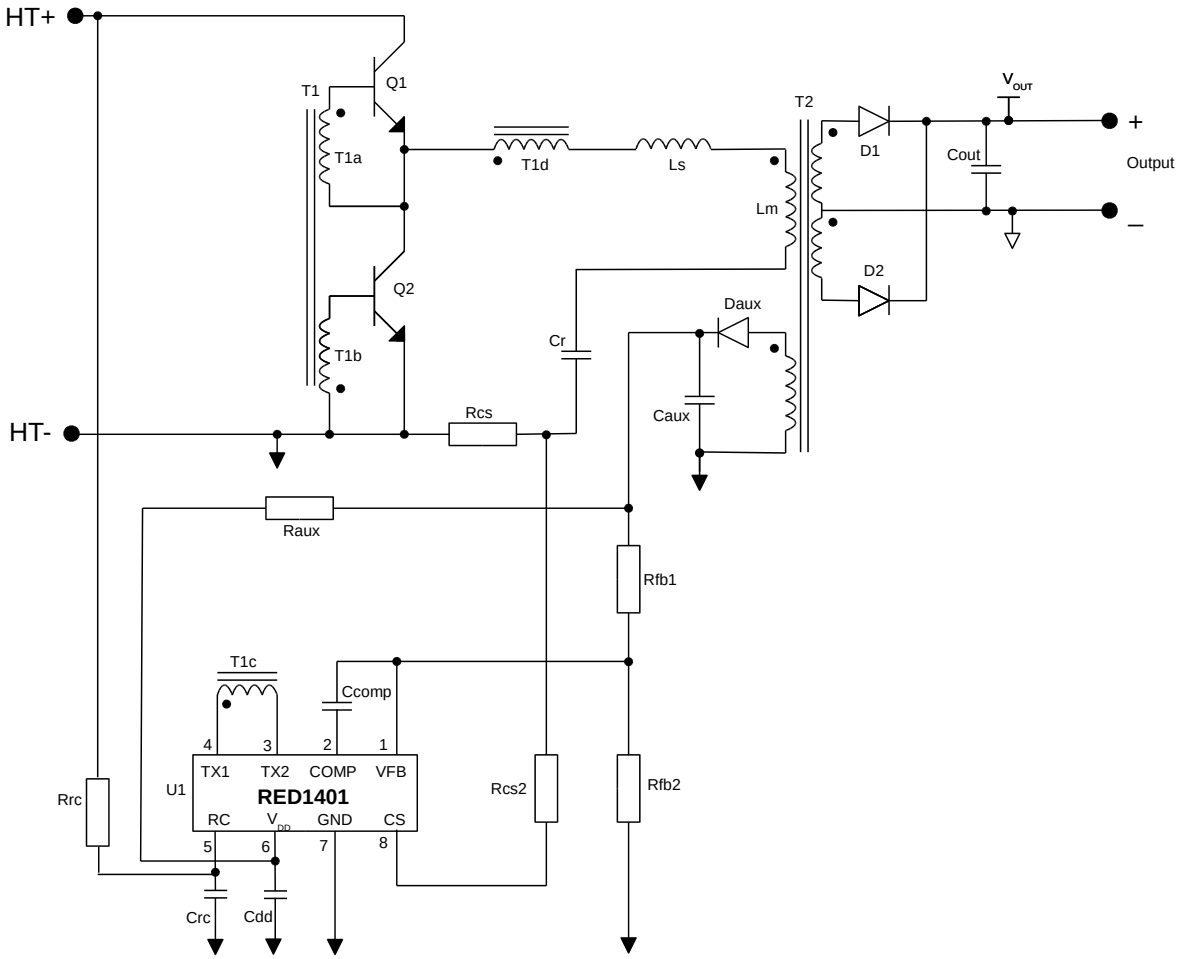


Figure 3: Typical Application Schematic: LLC converter with RED1401 PSR controller

Features

RED1401 is an advanced CMOS control IC for resonant LLC converters. The RED1401 Primary Side Regulation (PSR) control scheme removes the need for secondary side opto-coupler feedback, reducing cost and complexity.

RED1401 uses the CSOC (Controlled Self-Oscillating Converter) scheme to drive two low-cost bipolar transistors in a half-bridge configuration. RED1401 based LLC converters are able to achieve much higher efficiencies than similar flyback designs.

Accurate Primary Side Regulation

The RED1401 PSR scheme regulates the output voltage and current regulation by modulating the converter frequency. The PSR control is able to regulate output voltage off a primary-side sense winding. RED1401 enters controlled burst-mode operation at light loads to minimize the converter's input power consumption. The burst mode entry-point is preset by the PSR scheme to approximately 10% of the output current. The RED1401 PSR control is able to achieve <70mW standby in typical applications up to 30W.

Cable Compensation

To add to the accuracy of the primary side regulation technique, the IC also includes adjustable cable compensation. This enables more accurate PSR designs with using thin output cables.

Protection Features

The PSR control scheme also uses current sense input CS to provide constant current (CC) operation by frequency shift, long-term overload

(OVL) protection by delayed shutdown with automatic restart and instantaneous cycle-by-cycle over-current protection (OCP). The CC, OVL and OCP threshold levels are preset by the PSR control to provide excellent performance in typical applications.

The PSR control's Feedback Protection Feature (FBP) shuts down the controller if the feedback signal to the VFB pin is lost.

Over-temperature Protection

The RED1401 Over-temperature protection (OTP) feature shuts down the controller if the IC temperature exceeds 125°. The IC will restart the converter when the IC temperature drops by 20°C.

Automatic Dead-Time Control

An important feature of the CSOC (Controlled Self Oscillating Converter) is that the dead-time is controlled naturally. Unlike MOSFET half-bridge converters, it is not necessary to program the dead-time on RED1401. The bipolar switching transistors are turned on correctly through the self-oscillation of the converter and turned off by RED1401. This greatly simplifies the design process and improves the robustness of the LLC converter.

Capacitive Mode Protection

RED1401 includes a capacitive mode protection feature which prevents the converter from entering capacitive switching mode on a cycle-by-cycle basis by limiting the minimum frequency. This always ensures the Controlled Self Oscillating Converter (CSOC) continues to oscillate correctly and is therefore much more robust than MOSFET-based resonant converters.

IC Operation

Startup, Shutdown and re-start

Figure 4 shows typical startup waveforms for RED1401. In SLEEP mode the IDD current is approximately 8uA ($I_{DDSLEEP}$). Once VDD reaches 3.6V ($V_{DDSTART}$) the IC goes into RUN mode. The controlled Zener clamp inside the IC turns on and regulates the VDD voltage to 3.45V (V_{DDREG}). The IC current is now approximately 650uA (I_{DDREG}) plus any excess current required to clamp VDD to 3.45V. If VDD falls below 3.45V (V_{DDREG}) the Zener clamp turns off and I_{DD} reduces to 650uA (I_{DDREG}) only. If VDD falls by 570mV (ΔV_{DDSA}) below V_{DDREG}, the IC tries to keep itself alive by entering RUN mode and issuing start pulses. If VDD falls by 1.05V ($\Delta V_{DDSLEEP}$) below V_{DDREG}, the IC enters SLEEP mode. In this condition I_{DD} reduces to 8uA ($I_{DDSLEEP}$).

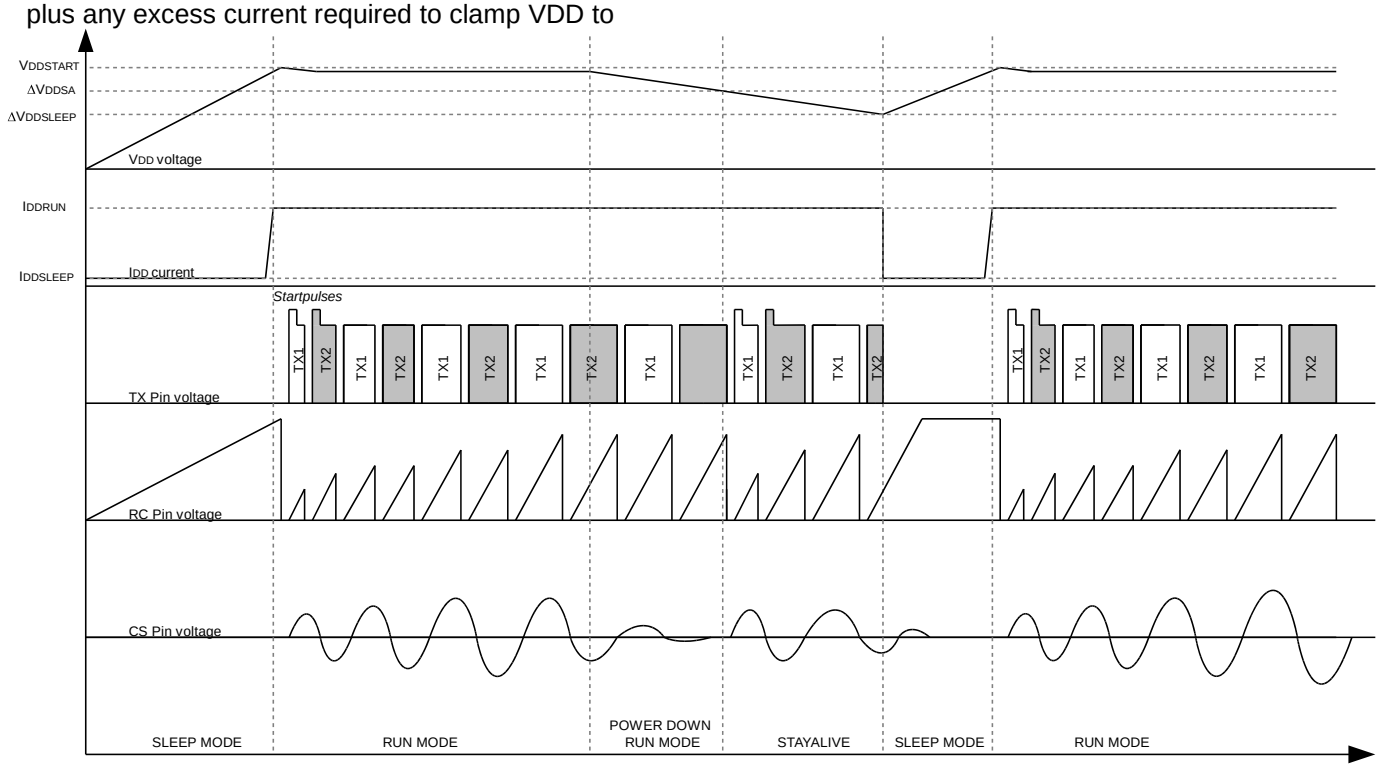


Figure 4: IC Start-up waveforms

Output stage

A diagram of the output stage can be seen in Figure 5. To start the converter oscillating the RED1401 issues start pulses through the TX1, TX2 pins during the first two cycles. These start pulses are 700ns long ($t_{TXSTART}$) and provide 8mA ($I_{TXSTART}$) current pulses from both TX1 and TX2 pins. After this the converter self-oscillates and no longer needs start pulses to maintain oscillation. A low on-state NMOS transistor is used to turn the bipolar transistors off. It is controlled by the oscillator off-time. The NMOS device is turned to pull TX1 or TX2 pin low, which switches off the corresponding bipolar transistor in the power converter half-bridge.

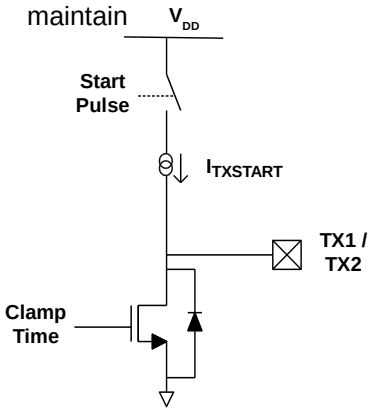


Figure 5: Output Stage

PSR Voltage and Current Regulation

The output voltage and current are estimated by the RED1401 PSR scheme. Inside the IC there are two separate control loops that control the converter output voltage (in CV mode) and the output current (in CC mode). The RED1401 regulates the output voltage and output current by controlling the frequency. A control voltage (V_{COMP}) is fed into the oscillator to give the desired operating frequency. Figure 6 shows how the two voltage and current error amplifiers and their compensation networks are configured for a primary regulated resonant converter.

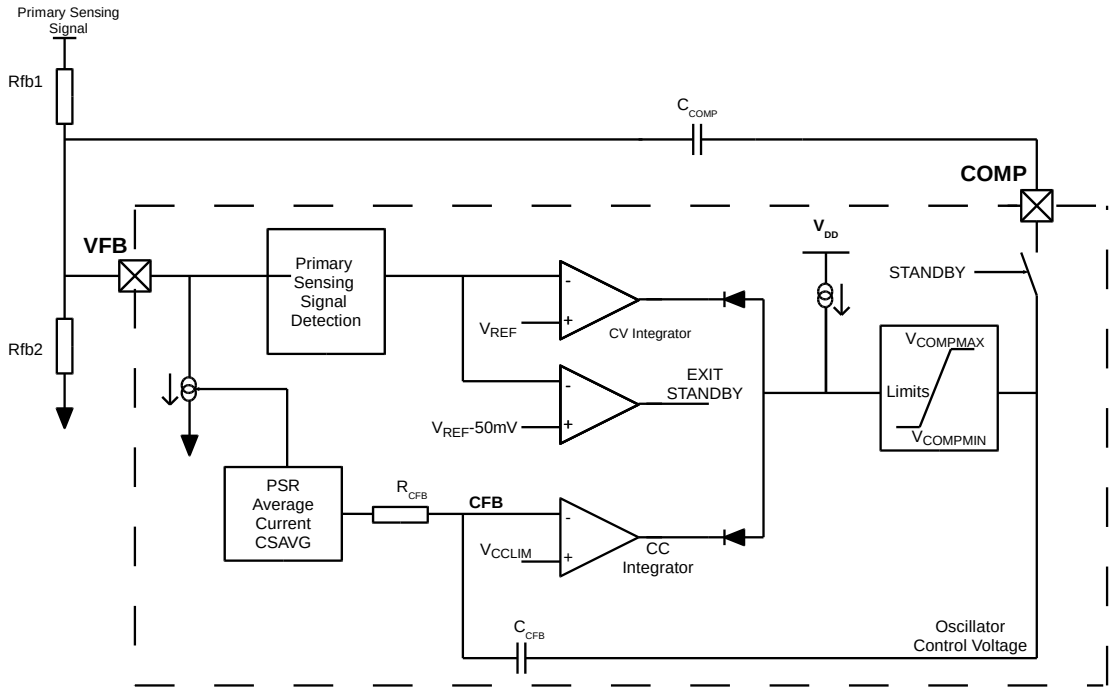


Figure 6: Error Amplifier Circuits

PSR Voltage Compensation Loop

The feedback network between the COMP and VFB pins defines the loop gain and phase for the voltage control loop. For Primary Side Regulation (PSR) this network should be configured to form an integrator with lead compensation and some high-frequency noise suppression. The VFB input senses the output voltage from an auxiliary winding on the primary side of the transformer. This signal is conditioned in the PSR block and compared to a fixed voltage reference of 1.2V (V_{REF}) inside the IC.

In normal operation (i.e. not in standby) the internal COMP signal is connected to the COMP pin.

In standby mode, the external compensation network is disconnected from the COMP pin and the PSR control remembers the previous value of COMP. This is explained more in the standby section.

Cable Compensation

Cable compensation is implemented with the VFB pin. An internal current sink proportional to the load current is connected to the VFB pin. With zero load on the converter, no current is drawn while at 100% load 4.5uA (I_{VFB}) is drawn into the VFB pin.

The effect of sinking current into the VFB pin is to reduce the VFB feedback voltage so that the RED1401 voltage error amplifier compensates for this by increasing the output voltage. The cable compensation loop is internal to RED1401 and has a much slower response than the external voltage control loop to avoid interference between the two control circuits.

The desired amount of cable compensation is set by choosing the impedance seen by the VFB pin. To disable cable compensation set the value of the resistor between VFB and GND to 5k. In a low power application with a thin output cable, choose a resistor value of approximately 25k.

Current Protection & Control Methods

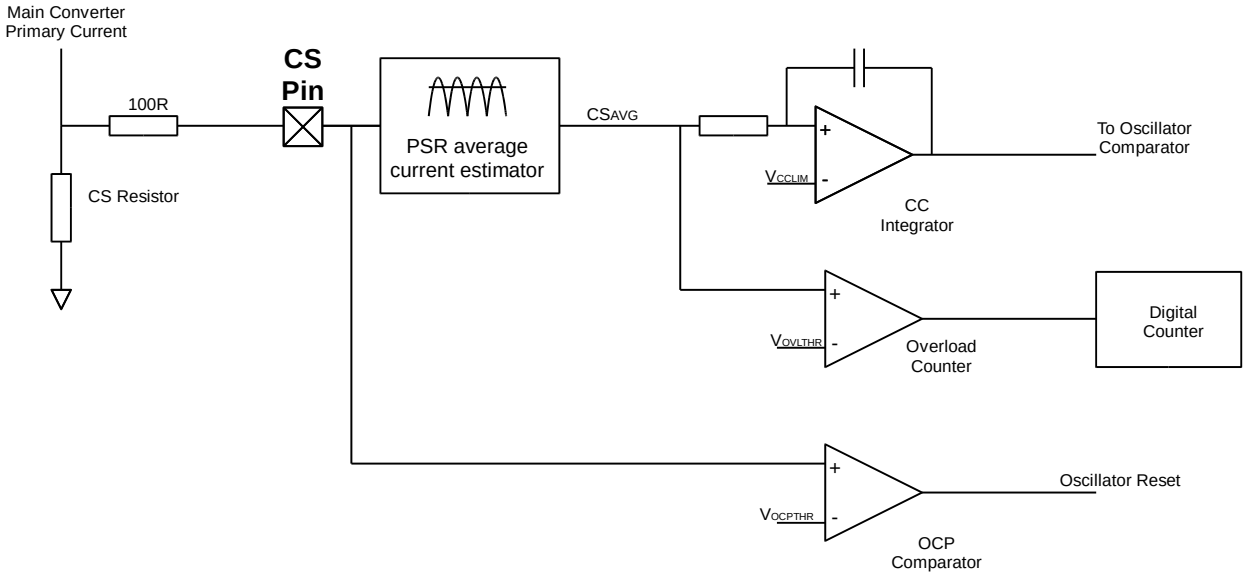


Figure 7: RED1401 Current protection and control circuits

Figure 7 shows the three current protection methods used in the converter:

1. a short-term constant current (CC) limit;
2. a long term current overload (OVL) shutdown;
3. an instantaneous peak current limit (OCP).

PSR Average current estimation

Shown in figure 7 the signal from the CS pin is divided into two different paths. The bottom path provides peak instantaneous over-current protection (OCP) while the PSR Average Current estimation block provides the current limit (CC) and the average current overload (OVL) information. The voltage on the CS pin is an AC signal biased around GND. Inside the PSR block this signal is processed to provide a voltage proportional to the average converter output current.

Constant Current Limiting

The CC limiting circuit is shown in Figure 7. The CC operation is defined by an internally compensated control loop. This provides a system response time of approximately 1ms in a typical SMPS application. The constant current RMS limit, V_{CCLIM} is pre-set to 140mV, referred to the CS pin. This corresponds to 140% of nominal load.

Average current overload

The average current signal (referred to the CS pin) is compared to a threshold level of 125mV (V_{OVLTHR}). A characteristic of the LLC converter is that the magnetising current changes significantly with frequency which can result in a significant error on the average current signal. To compensate for this, the PSR control dynamically adjusts the overload threshold voltage V_{OVLTHR} depending on the operating frequency. This corresponds to 120% of nominal load. The overload counter is a bi-directional counter that counts up when the converter output current exceeds this limit and counts down when the converter current is lower than the limit. Once the cumulative count of ups and downs equates to 16384, the RED1401 goes into SLEEP mode and the converter shuts down.

After 8 dummy restart attempts, (typically 2s) the converter will re-start again. RED1401 initiates the start-up sequence and issues start pulses to start the converter up as normal. If the overload persists, the converter will shut down again, but if the overload has been removed, the converter will continue operating normally.

Over Current Protection

Over-Current Protection (OCP) is an instantaneous termination of the transistor on-time. When a peak voltage greater than +/-500mV (V_{OCPTHR}) is sensed on the CS pin the OCP comparator terminates the current oscillator on-time cycle. The oscillator is reset and the off-time begins resulting in the bipolar transistors turning off and the half-bridge commutating. This is repeated in subsequent cycles whenever the CS voltage exceeds the threshold. However, in a correctly designed converter it should not be possible to trip OCP in normal operation.

Oscillator

The oscillator (see Figure 8) controls the period of a converter half-cycle. Internal to the IC is an oscillator comparator that compares the voltage on the RC pin to the voltage on the COMP pin. The RC pin has a saw tooth type waveform and the COMP signal should have a steady voltage, inversely proportional to the required frequency.
The COMP pin voltage can vary from 0.55V ($V_{COMPMIN}$) to 2.35V ($V_{COMPMAX}$), resulting in a maximum to minimum frequency ratio of approximately 3 for any input voltage.

The timing capacitor C_{RC} may be chosen within the range 90 – 470pF. The recommended type is a 150pF 5% COG/NPO capacitor.
The oscillator timing resistor R_{RC} may be connected to either V_{DD} or to the rectified DC bus, V_{HT}. If connected to V_{DD}, the value of R_{RC} may be calculated using following equation.

$$F_{MIN} = \frac{1}{2\left(0.7us + R_{RC}.C_{RC}.\ln\left(1 - \frac{2.35}{3.45}\right)\right)}$$

This equation gives the lowest possible operating frequency of the converter.

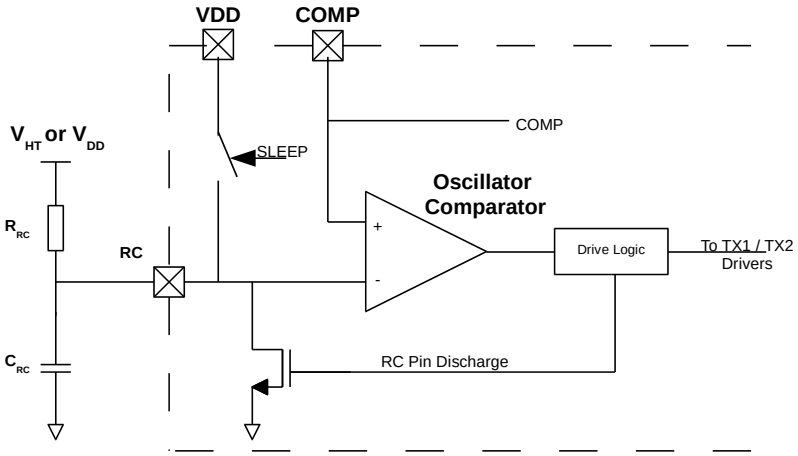


Figure 8: Oscillator circuit

Oscillator Feed-forward Compensation

The oscillator may optionally include feed-forward compensation. Feed-forward compensation is recommended to minimise the line frequency voltage ripple on the output, particularly for off-line applications where the DC bulk supply is unregulated. To apply the feed-forward compensation, the oscillator pull-up resistor R_{RC} is connected to the DC bulk supply V_{HT} instead of V_{DD}. The value may be calculated as a function of the DC bulk voltage using the following equation:

$$F_{MIN} = \frac{1}{2(0.7us + R_{RC}.C_{RC}.2.35/V_{HT})}$$

To assist feed-forward applications, a switch is provided which connects the VDD pin to the RC pin while the controller is in SLEEP. This allows the R_{RC} resistor to pull up the VDD supply for startup.

Standby

The IC enters controlled burst-mode operation at light loads, thereby minimising the converter's input power consumption.

Standby Entry

RED1401 enters standby when the IC reaches its maximum allowable operating frequency or when a low load condition is detected. The circuit that forces the IC into standby is shown in Figure 9.

When the output load current is low, the PSR average current estimate falls below a pre-set Burst comparator threshold. This is how the IC enters standby in a typical application. The Burst threshold is set to around 10% of full load and is compensated for varying input voltage. If the converter's load drops below 10% RED1401 will enter standby which temporarily turns the converter off to reduce overall application standby power.

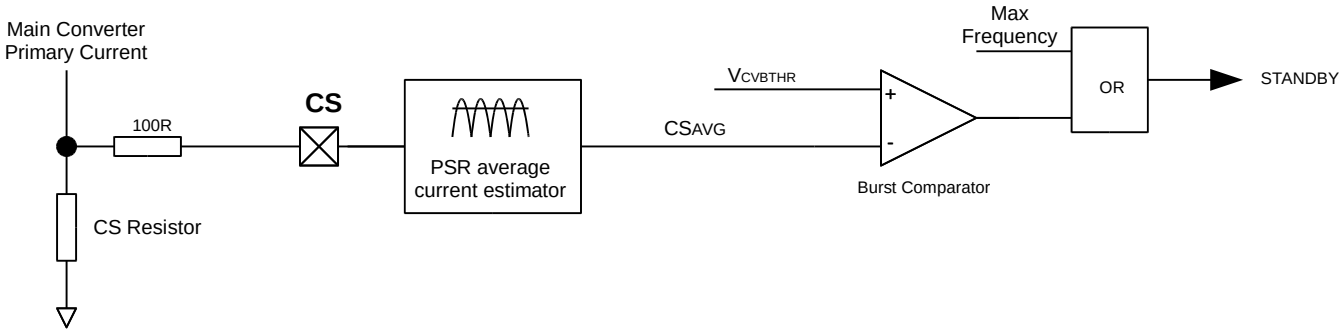


Figure 9: standby entry circuit

Standby Exit

When the IC enters standby, load is normally low and the RED1401 is operating at a high frequency. In standby the external loop compensation circuit is disconnected and the value of COMP is stored by the PSR circuit. When the voltage on the VFB pin falls by 100mV ($\Delta V_{EXITSBY}$) the RED1401 exits standby and enters RUN mode. The converter will deliver power to the load again and the IC will remain out of standby until the load current falls below the 10% threshold, causing the IC to re-enter standby.

In standby, the burst frequency can be set externally by choosing the correct C_{aux} (in Figure 3). A larger value of C_{aux} will reduce standby power, but will also reduce burst frequency and therefore increase output ripple in burst mode.

Feedback Protection

RED1401 includes a feedback protection feature that stops the converter if the PSR feedback signal to the VFB pin is lost. If the voltage on the VFB pin is less than 43mV (V_{VFBLOW}) for 64 consecutive cycles the IC goes into SLEEP mode and shuts the converter down, with both TX pins in the clamping state to preventing converter oscillation.

After 8 dummy restart attempts (typically 2s) the converter will re-start again. The IC issues start pulses and the converter starts up as normal. If the feedback fault persists, the converter will shut down again, but if the fault has been removed, the converter will continue operating normally.

UnderVoltage Protection

RED1401 includes an undervoltage protection feature that stops the converter if the controller is unable to maintain regulation due to low line input voltage. If the voltage on the COMP pin is at the maximum limit 2.35V ($V_{COMPMAX}$) for 16384 cycles the RED1401 enters SLEEP and shuts down.

After 8 dummy restart attempts, (typically 2s) the converter will re-start again. RED1401 initiates the start-up sequence and issues start pulses to start the converter up as normal. If the undervoltage condition persists, the converter will shut down again, but if it has been removed, the converter will resume normal operation.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Permanent damage may result if a device is subjected to operating conditions at or in excess of absolute maximum ratings.

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	V_{DD}		-0.5	4.0	V
Supply current	I_{DD}		0	10	mA
Input/output voltages	V_{IO}		-0.5	V_{DD} + 0.5	V
Input/output currents	I_{IO}		-10	10	mA
Junction temperature	T_J		-20	+125	°C
Storage temperature	T_P		-20	+125	°C
Lead temperature	T_L	Soldering, 10 s		260	°C
ESD withstand		Human body model, JESD22-A114		2	kV
		Capacitive Discharge Model		500	V

NORMAL OPERATING CONDITIONS

Unless otherwise stated, electrical characteristics are defined over the range of normal operating conditions. Functionality and performance are not defined when a device is subjected to conditions outside this range and device reliability may be compromised.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Minimum supply current	I_{DDMIN}		0.8	1.2	1.5	mA
Junction temperature	T_J		0	25	125	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise stated:

- Min and Max electrical characteristics apply over normal operating conditions.
- Typical electrical characteristics apply at $T_J = T_{J(TYP)}$ and $I_{DD} = I_{DDREG(TYP)}$.
- The chip is operating in RUN mode.
- Voltages are specified relative to the GND pin.

VDD Pin

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	$V_{DDSTART}$	To enter RUN mode	3.2	3.6	4.0	V
	V_{DDREG}	$I_{DD} < I_{DDSHUNT}$	3.3	3.45	3.6	V
	ΔV_{DDSA}	To trigger STAYALIVE signal		570		mV
	$\Delta V_{DDSLEEP}$	To enter SLEEP mode		1.05		V
Supply current	I_{DDREG}	In RUN mode, $VDD < V_{DDREG}$		650	800	µA
	$I_{DDSLEEP}$	In SLEEP mode		8	12	µA
	$I_{DDSHUNT}$	VDD shunt regulator max current			8	mA

VFB Pin

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VFB threshold voltage	V_{REF}	T_J= 0°C to 105°C, V_{DD}=3.45V	1.18	1.21	1.24	V
VFB Hysteresis voltage	$\Delta V_{EXITSBY}$	In standby mode	90	100	110	mV
Cable compensation current	I_{VFB}	At 100% load		4.5		µA
VFB Feedback Protection threshold voltage	V_{VFBLOW}		35	43	50	mV

CS Pin

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Overload protection threshold voltage	V_{OVLTHR}	V_{COMP}=1.8V – 120% load		125		mV
Constant current limit	V_{CCLIM}	140% load		140		mV
Instantaneous over-current protection threshold	V_{OCPTHR}			500		mV

RC Pin

Parameter	Symbol	Condition	Min	Typ	Max	Unit
External capacitor range	C_{RC}		90	150	470	pF
Oscillator Frequency Variation	$\Delta F_{RC}/F_{RC}$	T_J= 0°C to 105°C, C_{RC}=150pF, V_{DD}=3.45V, V_{COMP}= $V_{COMPMAX}$			4	%
Oscillator reset time	T_{RCRST}			0.7		µs
Overload trigger cycle count	N_{OVLT}	V_{CSAVG} > V_{OVLTHR}		16384		Cycles
Overload recovery cycle count	N_{OVLS}			8		Cycles

COMP Pin

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Source/Sink current	I_{COMP}		-70		+70	µA
Maximum COMP voltage	$V_{COMPMAX}$	V_{DD}=3.45V		2.35		V
Minimum COMP voltage	$V_{COMPMIN}$	V_{DD}=3.45V		0.55		V

TX1, TX2 Pins

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On-state resistance	R_{TXON}			1.5	2	Ω
TX pin clamp current	$I_{TXCLAMP}$	TX pin frequency >30kHz			800	mA
Start-pulse output current	$I_{TXSTART}$			8		mA
Start-pulse width	$T_{TXSTART}$			700		ns

*Over-Temperature Protection (OTP)**

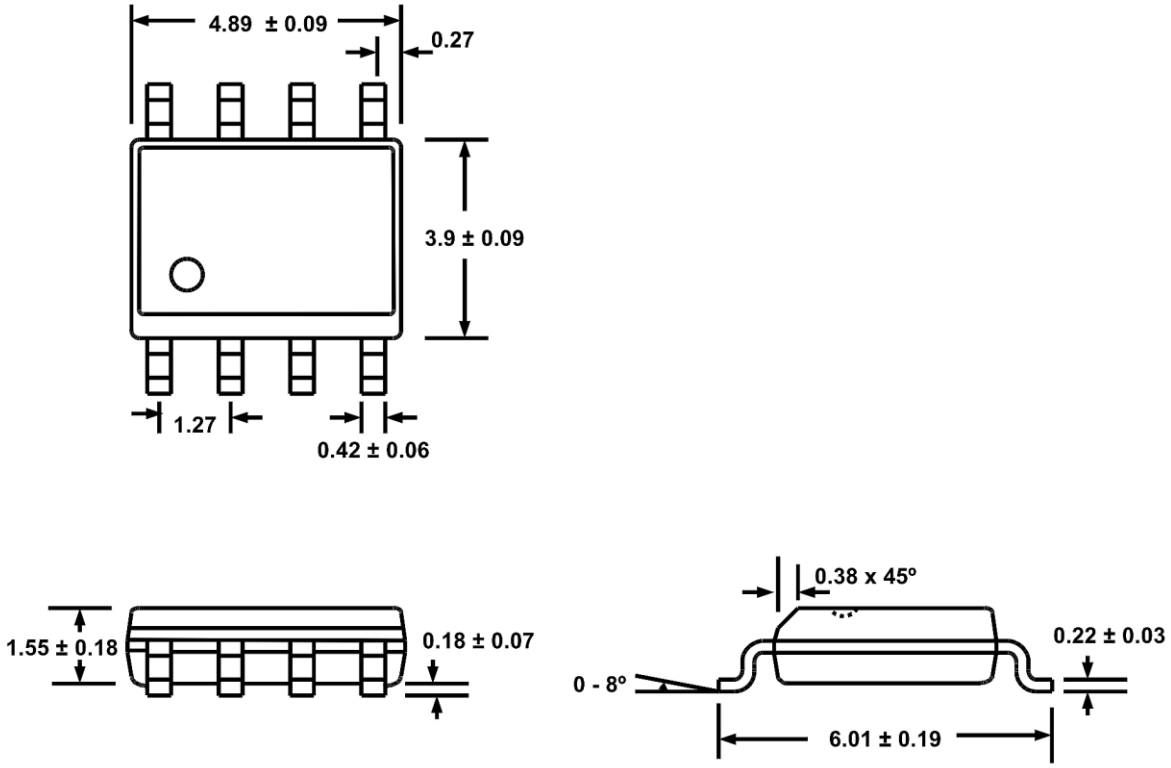
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Over-Temperature Protection threshold	T_{OTPS}	At silicon junction	115	125	135	°C
Over-Temperature Protection reset hysteresis	T_{OTP_HYS}	At silicon junction		20		°C

***: not tested in production*

PACKAGE INFORMATION

Package Dimensions

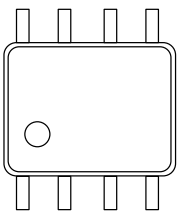
SO8 package dimensions are shown below. All units are in mm.



Available packages

Package type	Part number	Moisture Sensitivity Level (MSL)	Packaging	Thermal Resistances		
SO8	RED1401AD-TR13	3 (JEDEC J-STD-020)	Tape and reel 2500pcs/13" reel	Junction - Lead	θ_{JL}	30°C/W
				Junction - Ambient	θ_{JA}	150°C/W

Package Marking



RediSem
RED1401
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SO8 top-side marking for RED1401
RediSem = Manufacturer
RED1401 = Part Number
xxxx = Manufacturing Lot ID:

Lot ID explanation:
xxxx =0001, 0002...0099 Engineering Lot ID
xxxx =AA, AB, AC…ZZ Production Lot ID

Status

The status of this Datasheet is shown in the footer.

Datasheet Status	Product Status	Definition
Preview	In development	The Datasheet contains target specifications relating to design and development of the described IC product.
Preliminary	In qualification	The Datasheet contains preliminary specifications relating to functionality and performance of the described IC product.
Production	In production	The Datasheet contains specifications relating to functionality and performance of the described IC product which are supported by testing during development and production.

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